Talk Overview

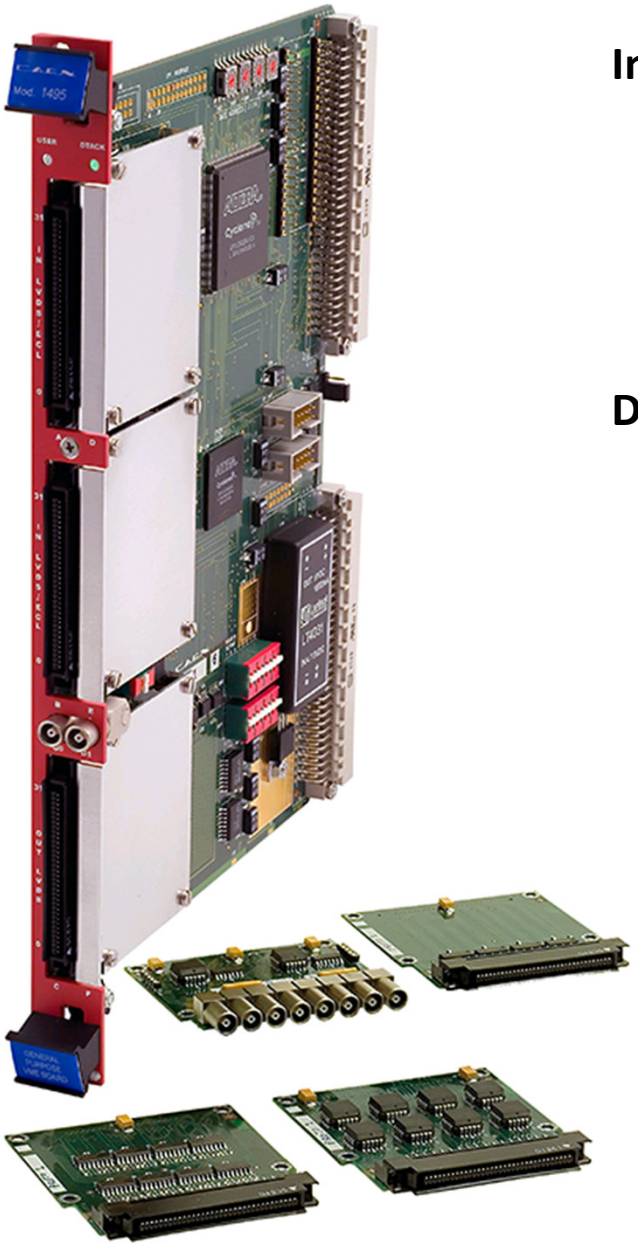
1. CAEN V1495 VME Module Overview

2. Example of completed V1495 projects at JLAB

3. Design tools/resources

4. Example V1495 project walkthrough

1.0 V1495 Overview



Input/Output Interfaces

- 64 dedicated differential inputs (LVDS, NECL, PECL)
- 32 dedicated outputs (LVDS)
- 2 bidirectional NIM ports
- 3 optional daughter card module slots

Daughter Card Modules

- A395D: 8 bidirectional NIM/TTL ports
- A395A: 32 differential inputs (LVDS, NECL, PECL)
- A395C: 32 ECL outputs
- A395B: 32 LVDS outputs
- A395E: 8 channel 16bit DAC (low speed)

1.1 V1495 Block Diagram

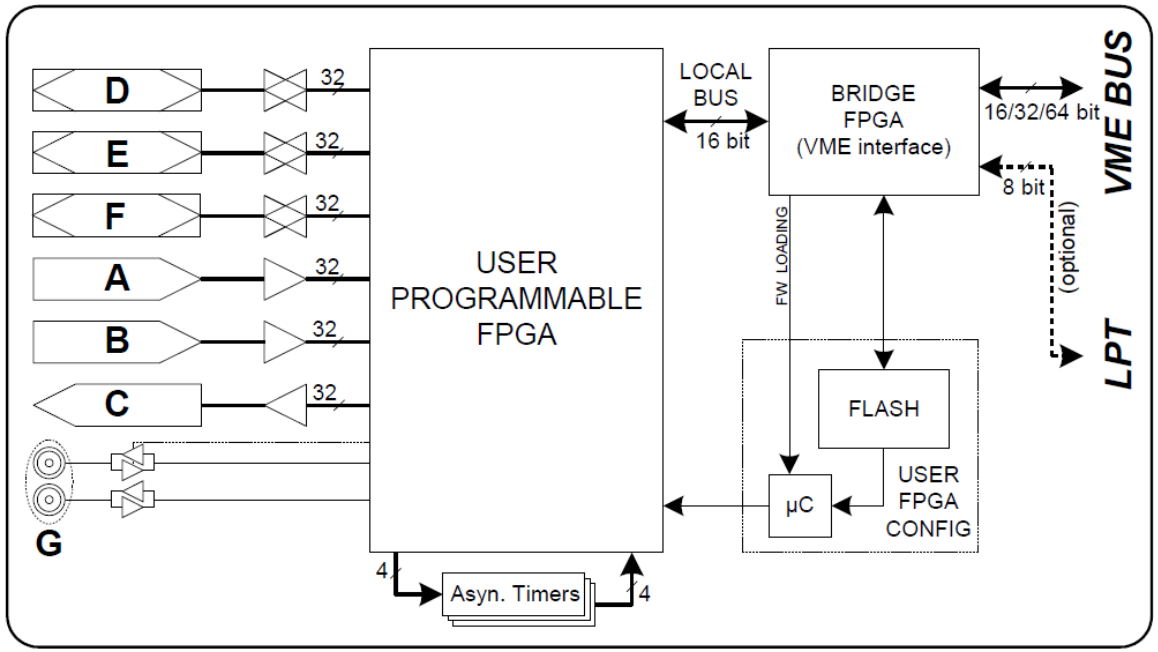


Fig. 1.1: Mod. V1495 Block Diagram

User programmable FPGA

- Custom user logic to interface all front-panel inputs/outputs
- VME bus has access to user logic (for parameter setup, status, event readout)
- VME interface provides 16/32bit single cycle accesses and supports only BLT32 for high speed readout
- FPGA firmware can be updated by user over the VME bus
- Onboard programmable delays for asynchronous delays

1.2 V1495 FPGA Resources

Altera FPGA: EP1C4F400C6

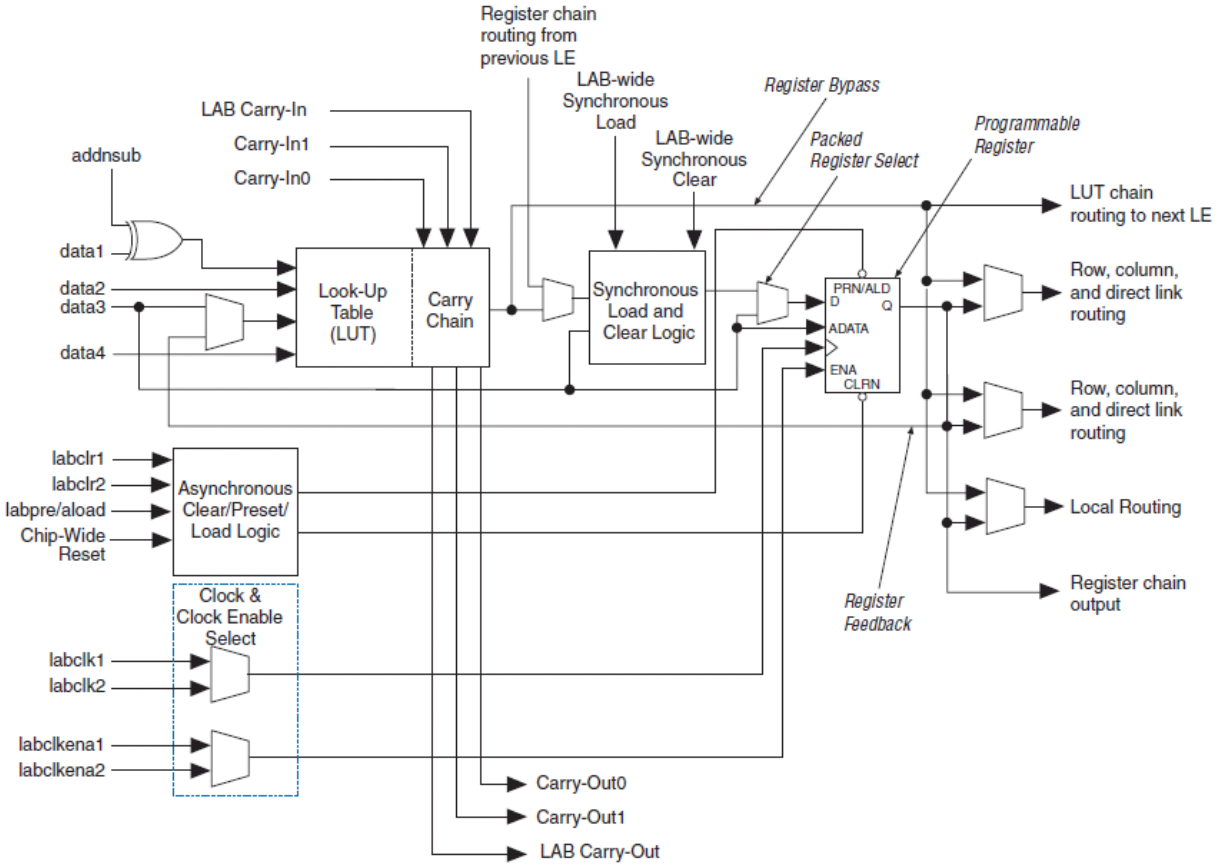
General features:

1. **FPGA Block RAM: 294912 bits**
   - Event buffering
   - Large delay lines
   - Histograms

2. **PLLs (2)**
   - Fast I/O sample rates (~200MHz)
   - Fast internal sequential logic (up to ~400MHz)
   - Synchronize multiple V1495 modules

3. **Logic Elements (LE): 20,060**
   - Counters, prescalers, small delay lines
   - Lookup tables
   - Combinatorial/sequential logic
   - Each LE contains a register/latch and 4 input LUT

1.3 V1495 FPGA LE



- The LE is the basic resource that most high level logic will be synthesized to use
- Software synthesizers will take high level code (state machines, counters, arithmetic operators, logic) and reduce them to utilitize the specific FPGA features
- The synthesizer is very good in general, but in some cases it needs help and can require user to understand the FPGA structure for high speed or density logic to work on the FPGA

2.0 V1495 Projects at JLAB

Hall B IC/Hodoscope Cluster Finder - Ben

Discriminator based 3x3 window calorimeter cluster finding.
(424 channels + 72 hodoscope)

Hall B Trigger - Ben

Hall B has been using the v1495 as the main trigger processor for the past few years. (sector/global trigger logic)

Hall A Signal Fanout – Ben

FastBus ADC and TDC testing board. Provided programmable delays and widths on many maskable ECL channels.

Hall C Compton Polarimeter (self-trigger, event readout) – Amrendra Nayaran

1-dimensional, multi-plane cluster finding for a diamond multi-strip detector.

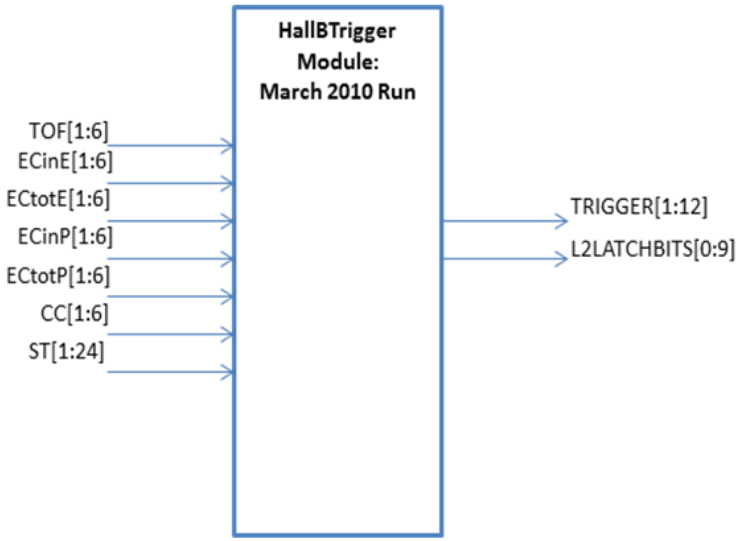
Hall C GEM Readout– Ben (eventually someone in QWEAK took this project over)

Provided triggered readout and buffering for 12 VFAT chips per V1495.

2.1 Hall B Main Trigger

HallB Trigger Module – Run March 2010 Description

Implemented on CAEN V1495 Programmable VME Module



6x Sector Inputs:

TOF, ECinE, ECtotE,
ECinP, ECtotP, CC, ST

Trigger Outputs:

12 Programmable, TRIG[1:12]
10 Bit Prescaler
0-35ns Pulse Stretcher

Programmable Delays:

All Sector inputs have individually controllable delays: 0 to 155ns in 5ns steps

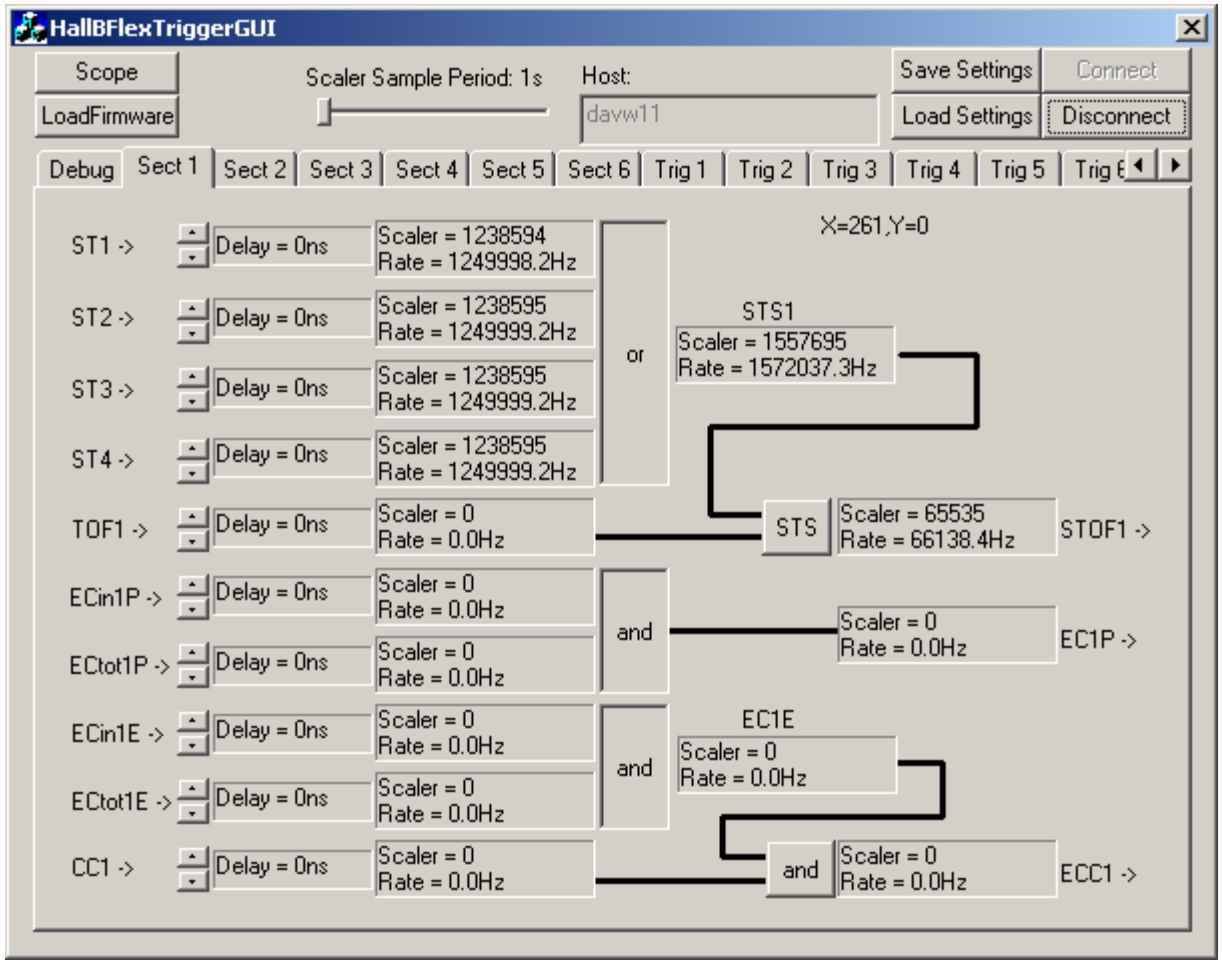
Trigger Output Jitter:

5ns

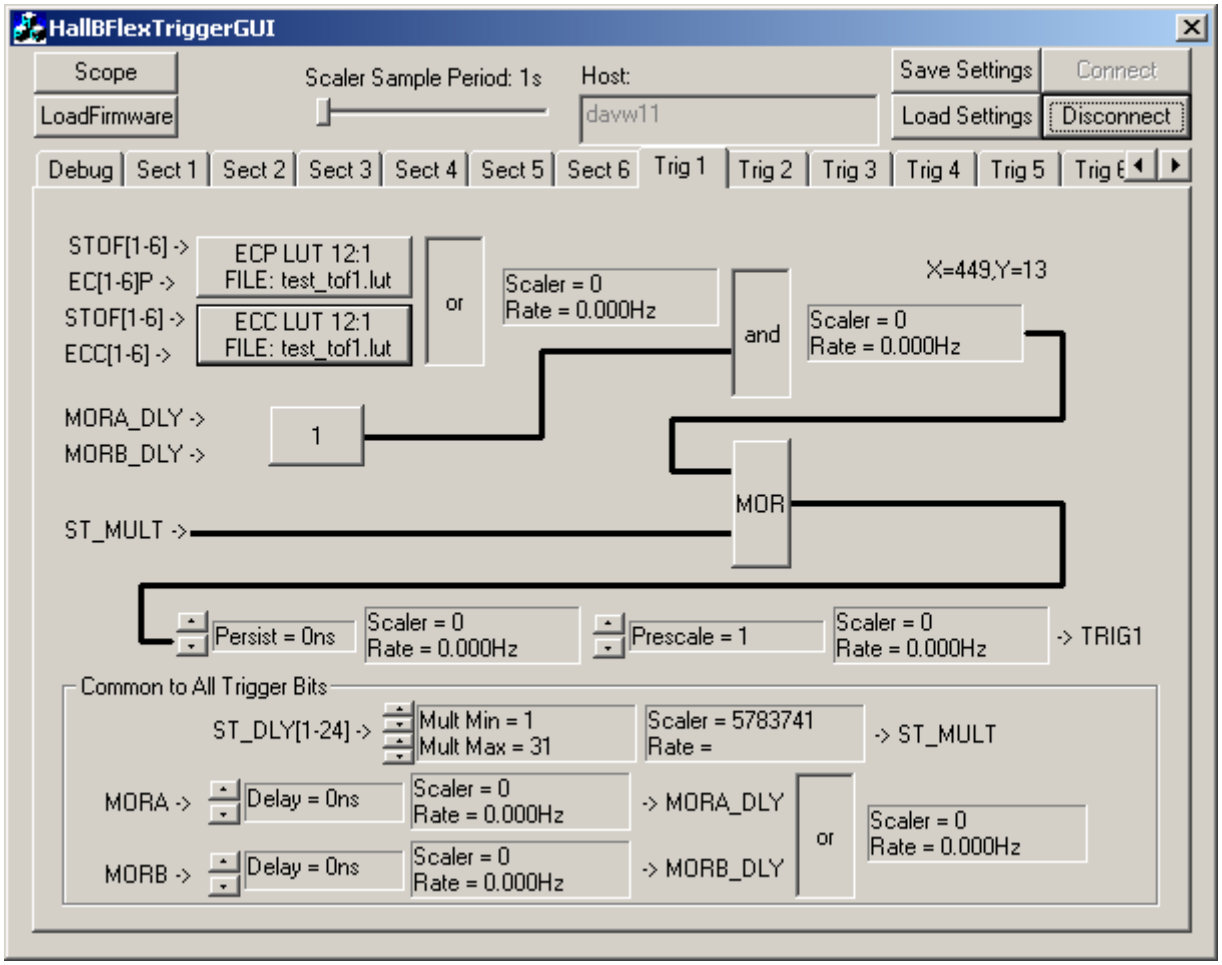
Scalars:

16/32bits 100MHz Count Rate
On all inputs, outputs, and most intermediate stages in trigger logic

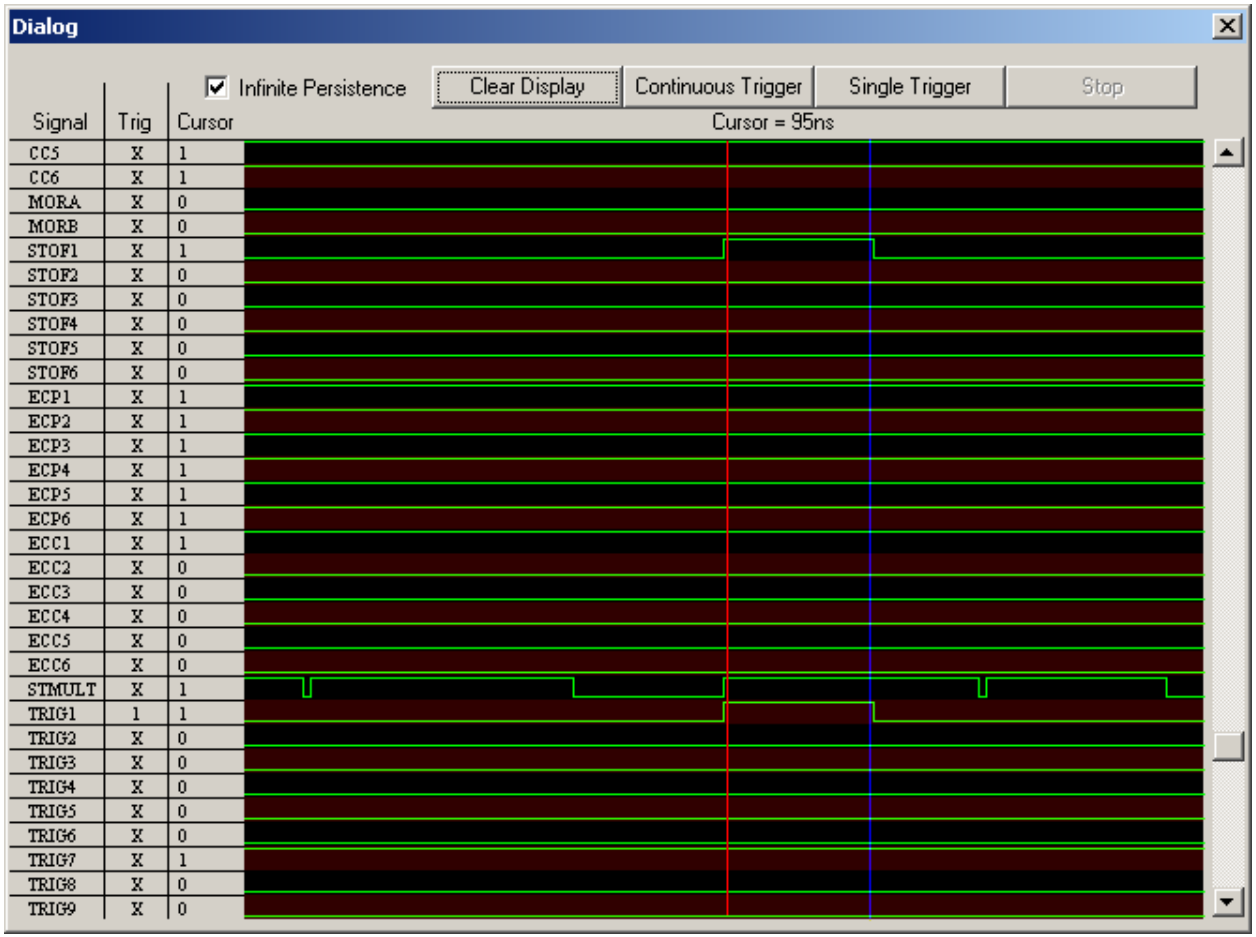
2.2 Hall B Main Trigger (sector triggers)



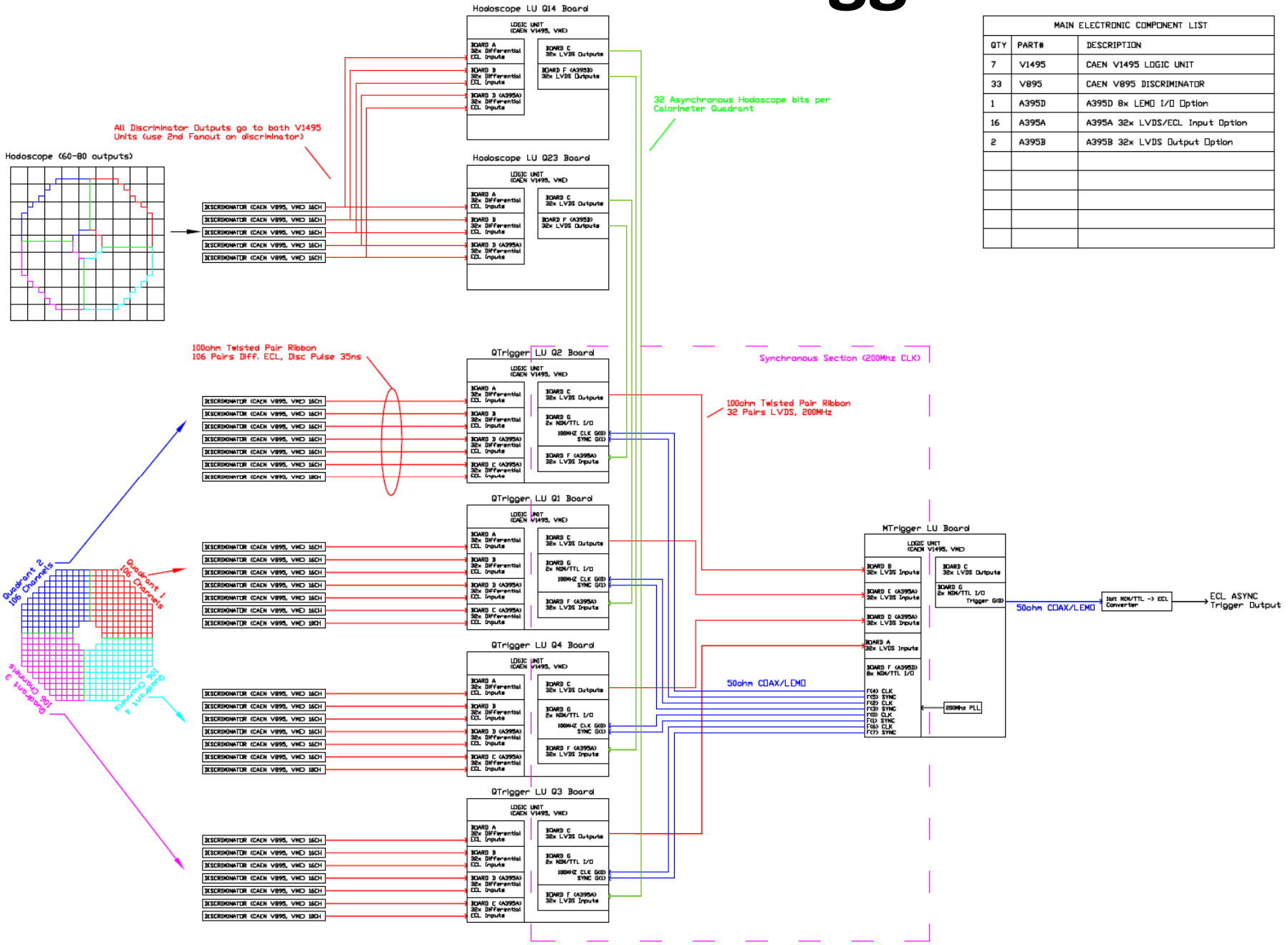
2.3 Hall B Main Trigger (global triggers)



2.4 Hall B Main Trigger (debug scope)



2.5 Hall B IC Trigger



MAIN ELECTRONIC COMPONENT LIST		
QTY	PART#	DESCRIPTION
7	V1495	CAEN V1495 LOGIC UNIT
33	V895	CAEN V895 DISCRIMINATOR
1	A395D	A395D 8x LEMO I/O Option
16	A395A	A395A 32x LVDS/ECL Input Option
2	A395B	A395B 32x LVDS Output Option

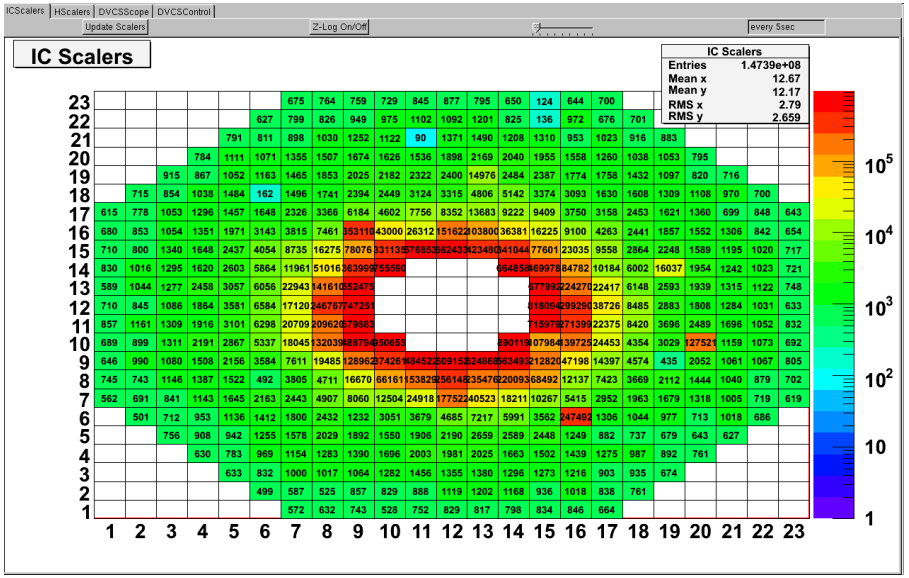
2.6 Hall B IC Trigger

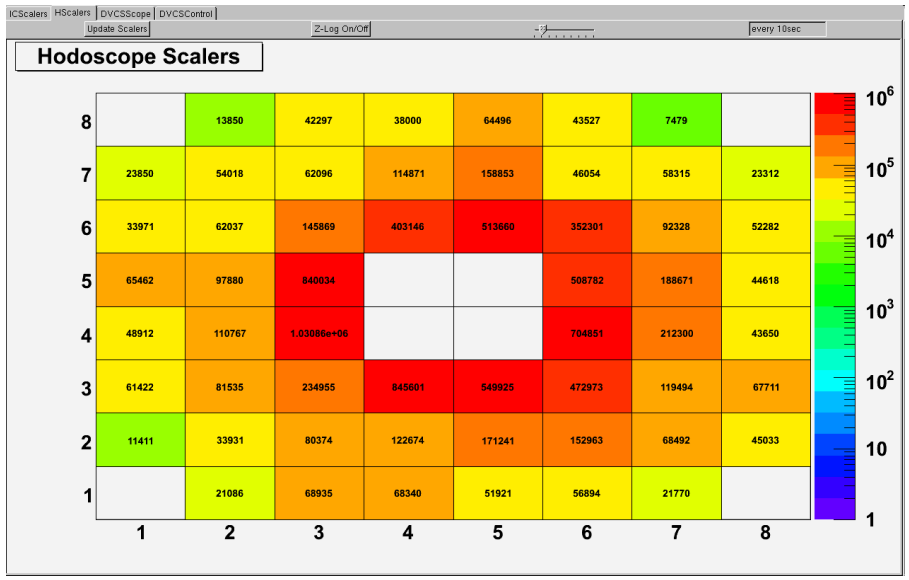
Embedded logic analyzer was developed for the 424 Channel Inner Calorimeter / 72 Channel Hodoscope in Hall B

- Cluster finding trigger implemented in multiple V1495 CAEN logic units. Scalers for all 496 channels & logic analyzer also embedded in trigger hardware.

- Trigger algorithm looked at all 3x3 window combinations of calorimeter searching for #hit towers to go above threshold to define cluster

- Hodoscope pixels were matched to IC cluster positions to identify charged/neutral clusters and provide counts to global trigger





2.7 Hall B IC Trigger

2D Logic Analyzer Details:

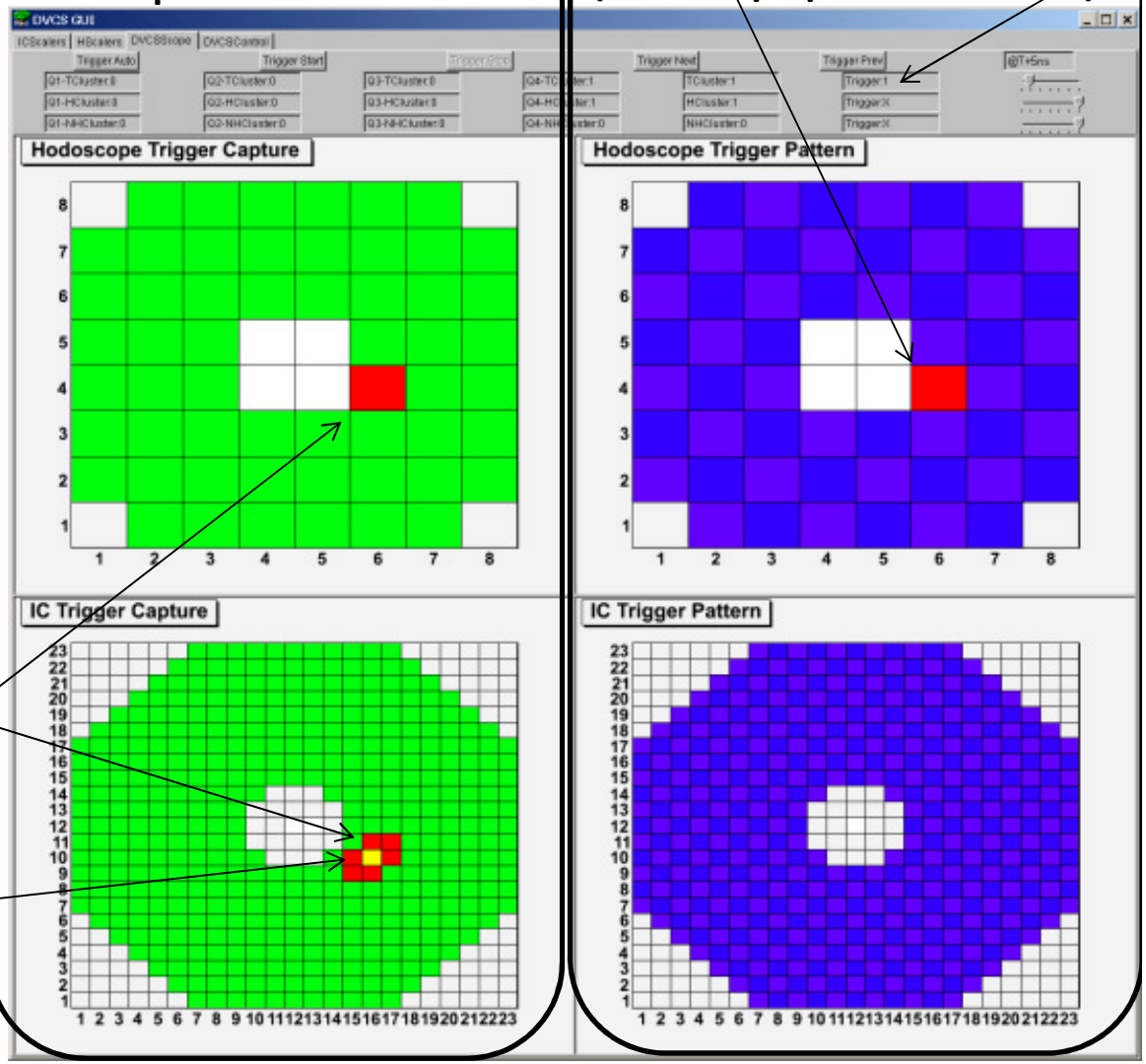
- Goal was to provide a remote debug interface to identify bad channels, verify cluster finding algorithm, check timing
- Logic analyzer runs in parallel, non-intrusive, to calorimeter trigger
- Can setup trigger on any IC/Hodoscope pixel arrangement and/or cluster count.
- After trigger, you can move forward/backward in time by ~250ns to see timing details

Geometric Match

Not Hit Tower/Pixel
Hit Tower/Pixel
Cluster Found
Don't care trigger

Triggered logic analyzer output:

Setup logic analyzer trigger (hodoscope pixel & 1 cluster):



3.0 Software & projects to download

Quartus II Web Edition (FPGA compiler-synthesizer/fitter):

Link: https://www.altera.com/download/dnl-index.jsp

Comments:

- Get version 9.1sp2 or 10.1sp1 (newer versions of free edition don't include support for Cyclone I series FPGA that's on the V1495
- Runs under Linux or Windows

Modelsim-Altera Starter Edition (FPGA simulation):

Link: https://www.altera.com/download/dnl-index.jsp

Comments:

- Get the version that matches the Quartus II Web Edition you have
- Runs under Linux or Windows

CAEN V1495 Example Projects:

Link: http://www.caen.it/csite/CaenProd.jsp?parent=11&idmod=484

Comments:

- Under "Software/Firmware" download all "v1495*demo*" files
- Under "Documentation" dowload "V1495 User Manual"
- These are CAEN example Altera Quartus projects for the v1495 that can be used as a basis to develop user specific designs for the v1495

3.1 Additional Resources

Recommended Design Practices (i.e. DO & DONTS for what kind of logic to implement on the FPGA):

http://www.altera.com/literature/hb/qts/qts_qii51006.pdf

Recommended HDL Coding Styles (i.e. how to write code to ensure the synthesizer can understand what you want):

http://www.altera.com/literature/hb/qts/qts_qii51007.pdf

VxWorks VME based firmware updater for 1495 (Intel version to come when needed)

Contact: braydo@jlab.org or boiarino@jlab.org

USB Blaster quick programming & debug tool:

- If think you'll be developing for the v1495, this tool pays for itself and more
- Get the generic one from Digikey (Digikey Part# P0302-ND) for $75
- This allows use of SignalTap for debugging your code while it runs in the board – a very powerful logic analyzer for debugging

4.0 Example Design Walkthrough

General Design Steps…

1) Breakdown the design into small modules (e.g. scalers, prescalers, delay line, memory, state machine, simple combinatorial logic, etc…)
2) Implement each module as a small, single entity (either VHDL, Verilog, Schematic)
3) Test each module using a dedicated testbench for each module that simulates (using Modelsim for example) as many features as possible (preferably all)
4) Build partial/full design out of these smaller modules and write a testbench to simulate this larger piece…
5) Once full design simulation is complete, compile (using Altera Quartus). Resolve timing/fitting problems (re-simulate any modified code)
6) Load compiled design into v1495 and test with real signals (can use SignalTap for debugging if needed)

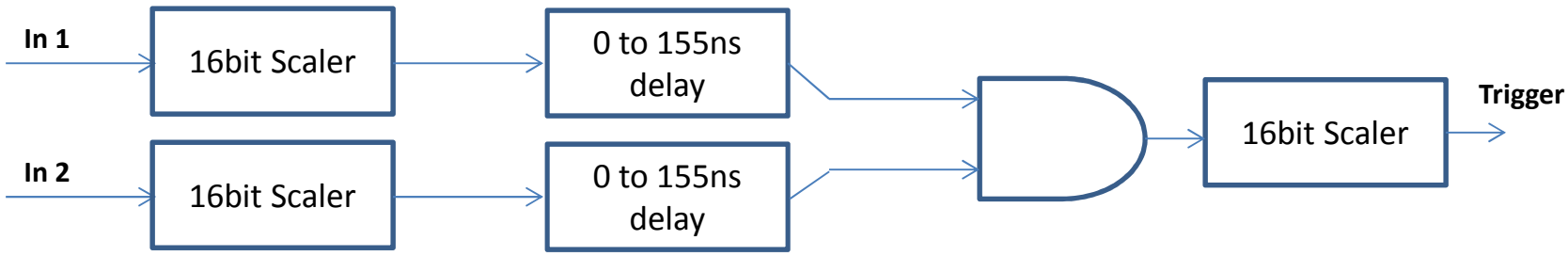
Modified files: Coin_reference.vhd,
V1495usr_pkg.vhd
-- B.R. modified (start)
-- B.R. modified (end)

Added files: Scaler.vhd, DigitalDelayLine.vhd,
PLLBlock.vhd, TriggerTestBit.vhd

4.1 Example Design

Example design:

- Form coincidence trigger signal from 2 inputs with unknown skew.
- Scalers on inputs and output signal
- Programmable delays on input signals to form coincidence by changing VME registers
- 200MHz clock sets sample rate, delay step size, and maximum scaler rates (200MHz/2)



4.2 Example Design

Starting from CAEN Coincidence Altera Quartus Project example:

V1495_User_Demo_QuartusII_Project_2_0-624.zip

I added the following files to the project:

Scaler.vhd	programmable scaler
DigitalDelayLine.vhd	programmable delay line
PLLBlock.vhd	200MHz PLL
TriggerTestBit.vhd	Example design
coin_reference_tb.vhd	Overall design testbech

I modified the following files:

V1495usr_pkg.vhd	Added new register addresses
coin_reference.vhd	Dropped in TriggerTestBit entity here, and update VME registes

…I put the following comments around the sections of the orignal CAEN project files that I modified:

```
-- B.R. modified (start)
-- B.R. modified (end)
```