Low level TOF signals

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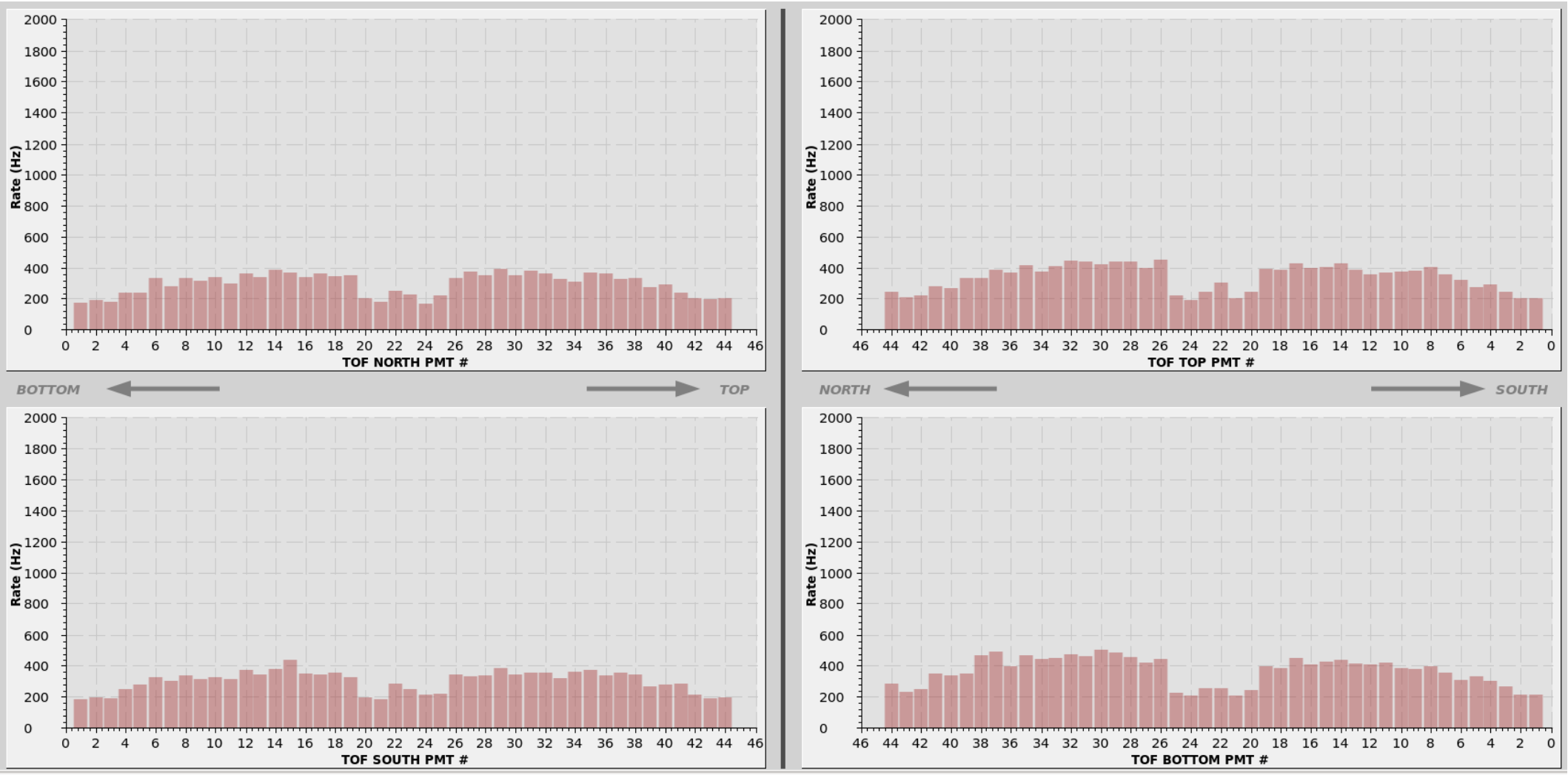
December 15, 2014

TOF discriminator scalers: No beam

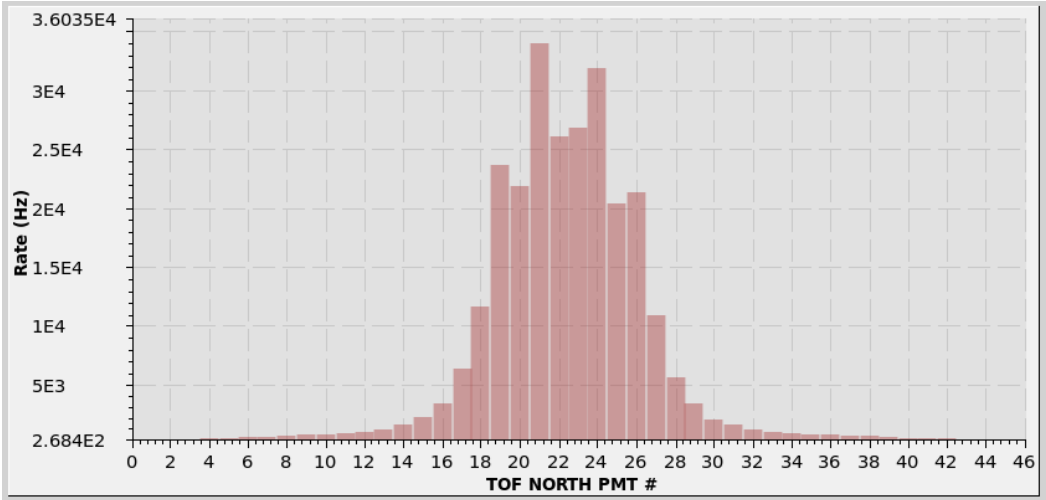
Range: 150 Hz – 500 Hz

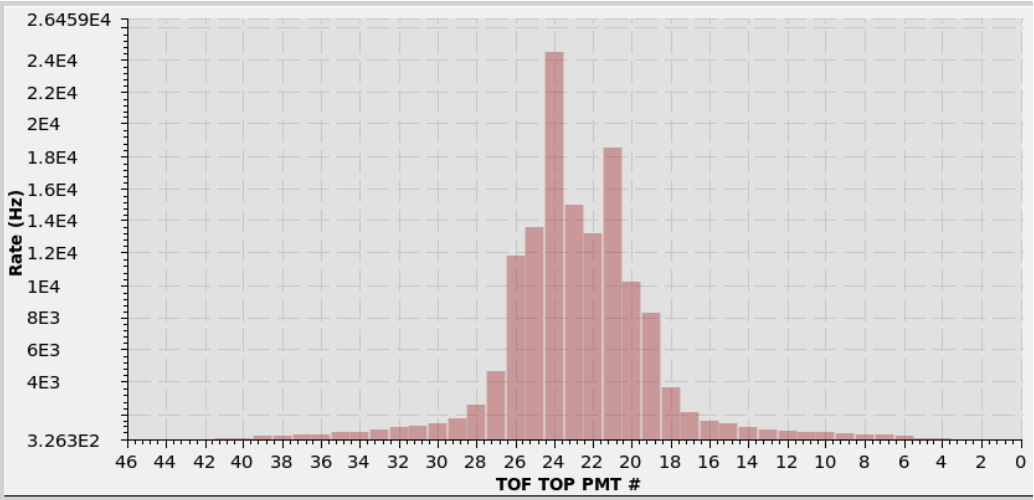


- Slightly higher rate closer to the beam line

TOF discriminator scalers: 50 nA, 2x10^{-5} radiator

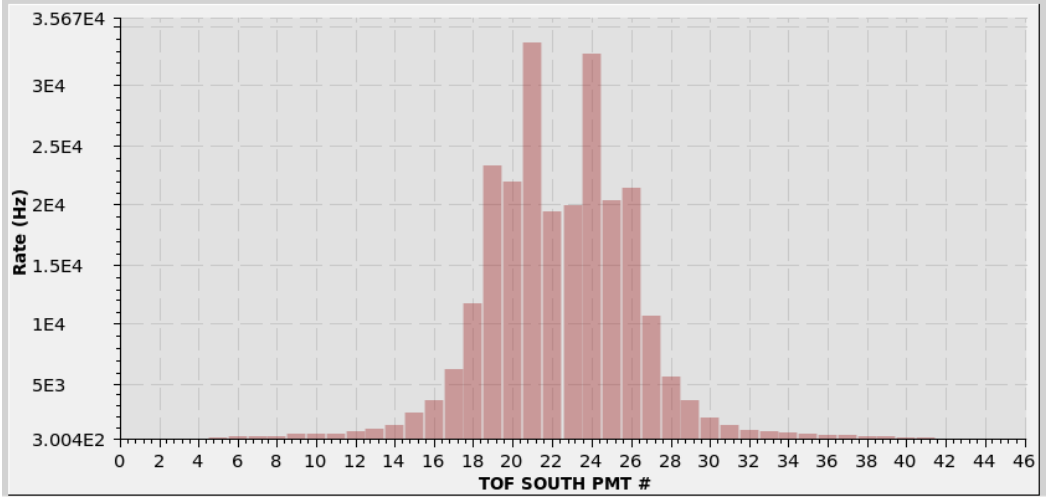
Rate up to 35 kHz at most common running condition

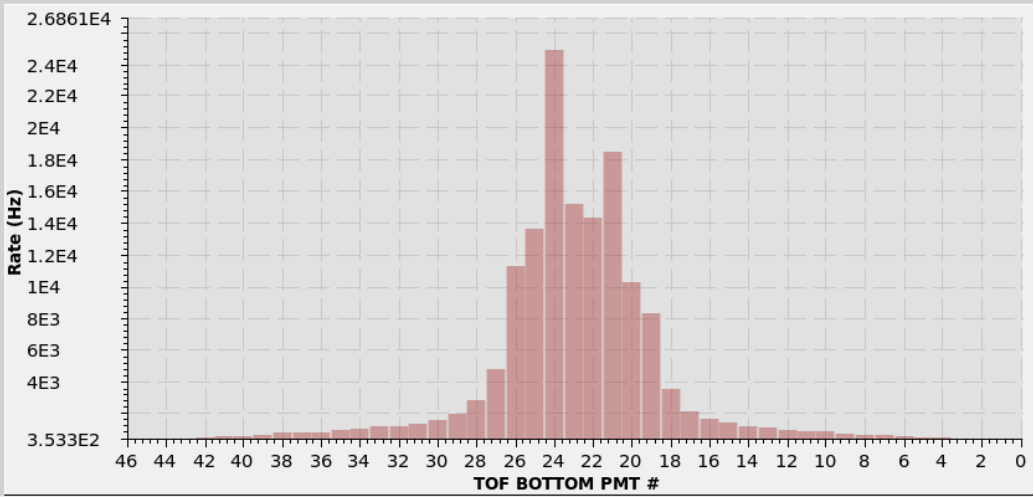




BOTTOM ← → TOP

NORTH ← → SOUTH

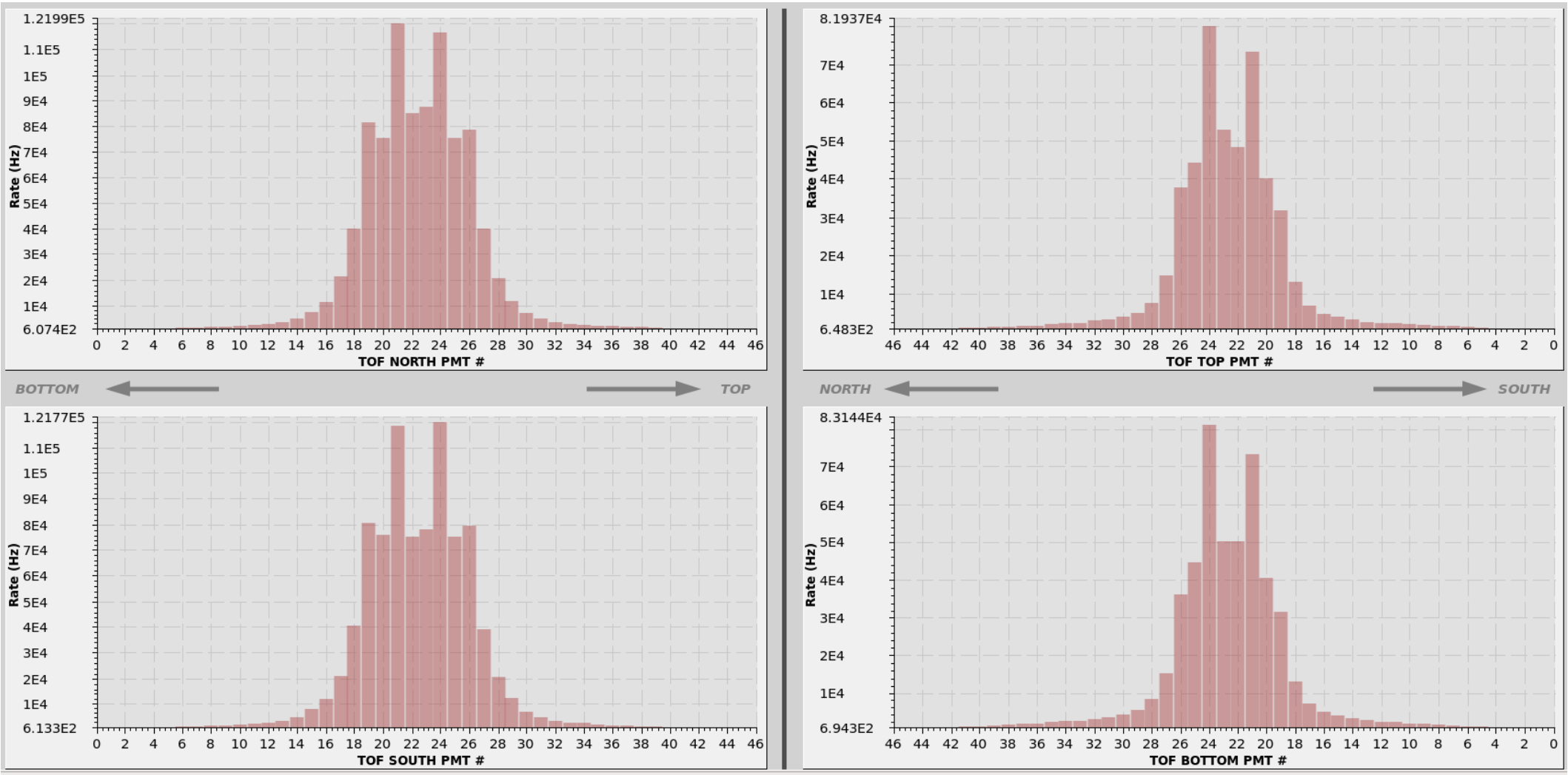




- Beam is slightly higher to the north (in agreement with ST scalers at that time)
- Upstream plane rate is about 50% higher than downstream plane

TOF discriminator scalers: 200 nA, 2x10^{-5} radiator

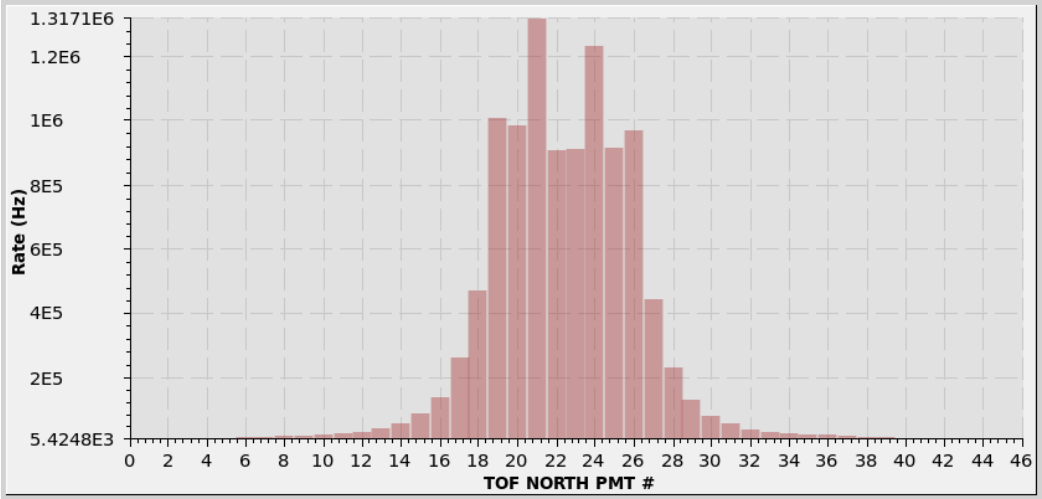
Rate up to 120 kHz

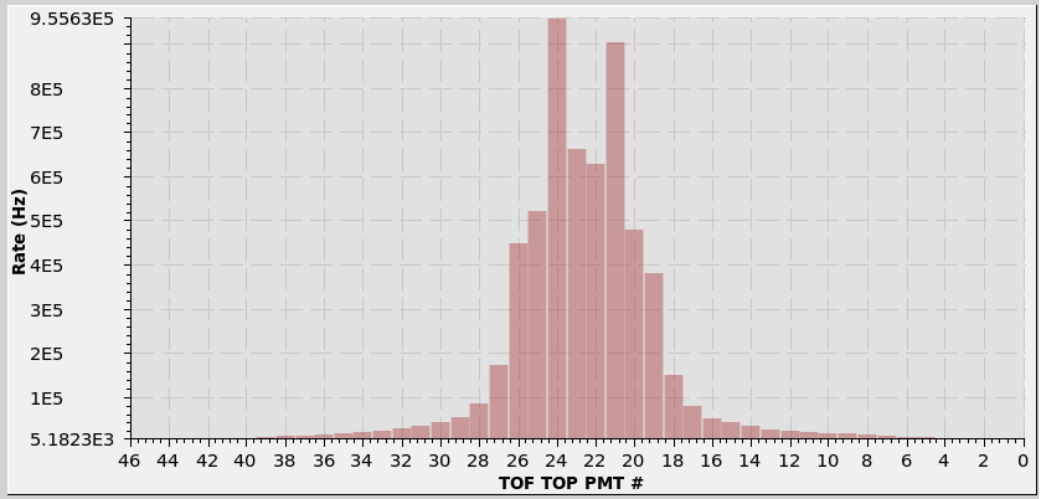


- With 4 times more current, rates are higher by a factor of 3

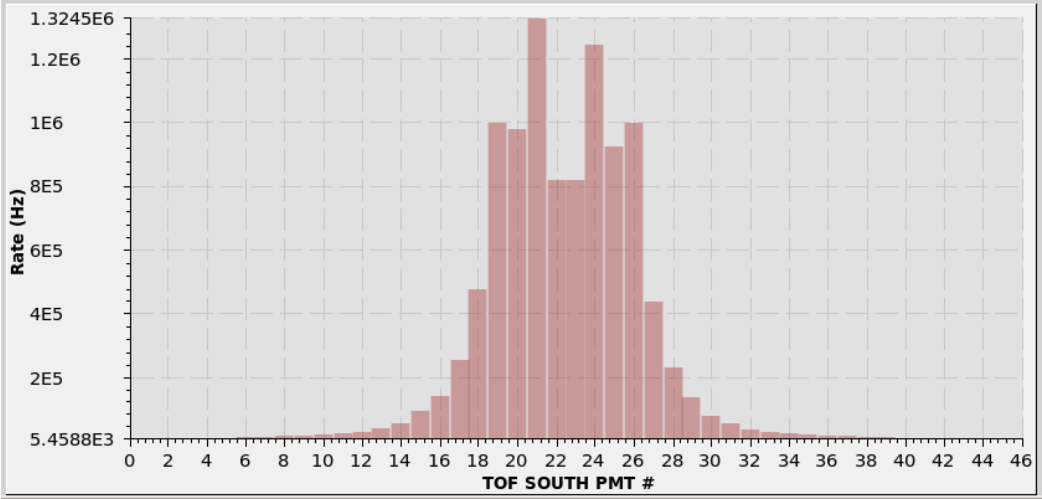
TOF discriminator scalers: 150 nA, 3x10^{-4} radiator

Rate up to 1.32 MHz at the highest tested luminosity (expected in spring 2015)

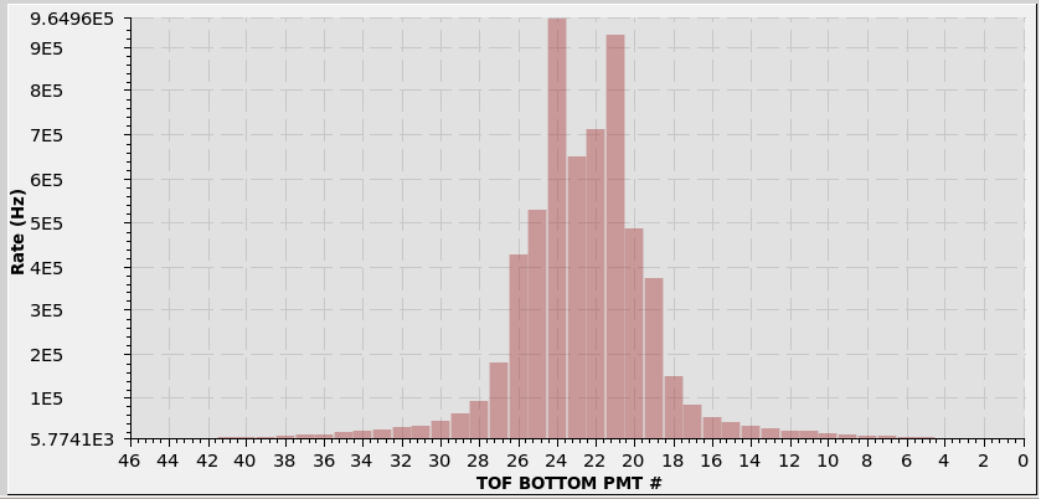




BOTTOM ← → TOP

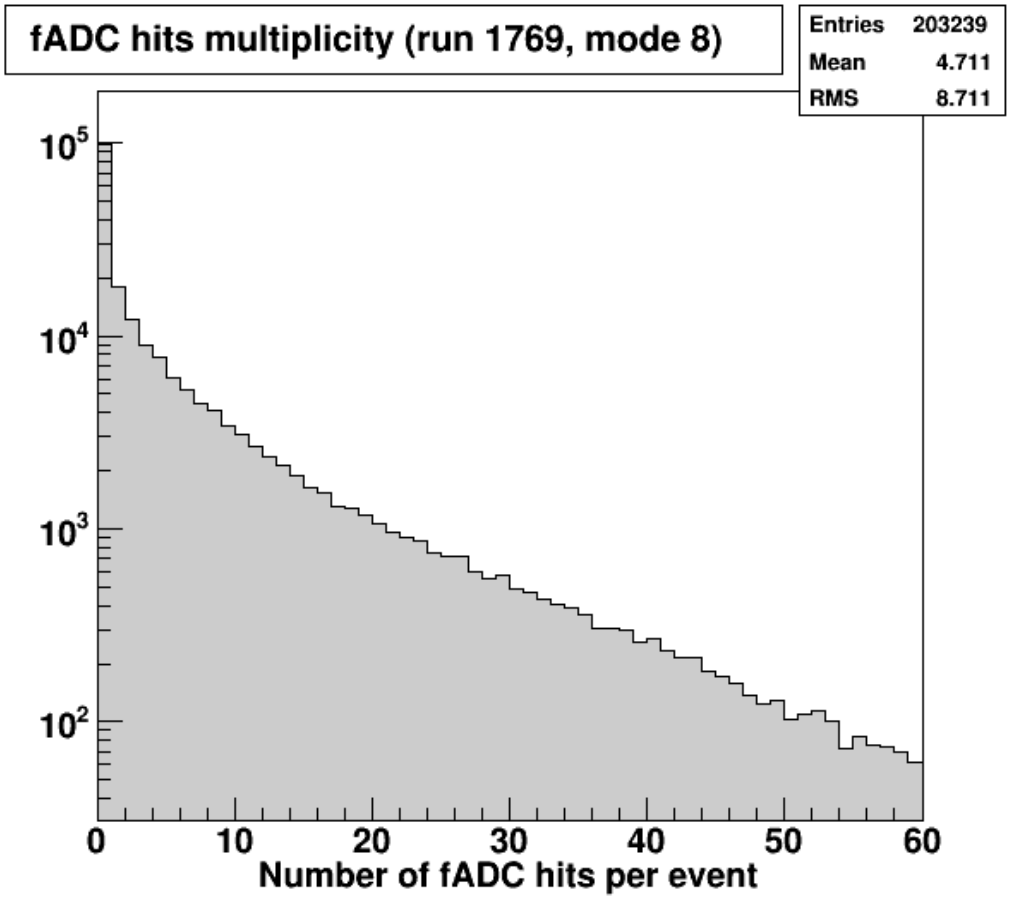


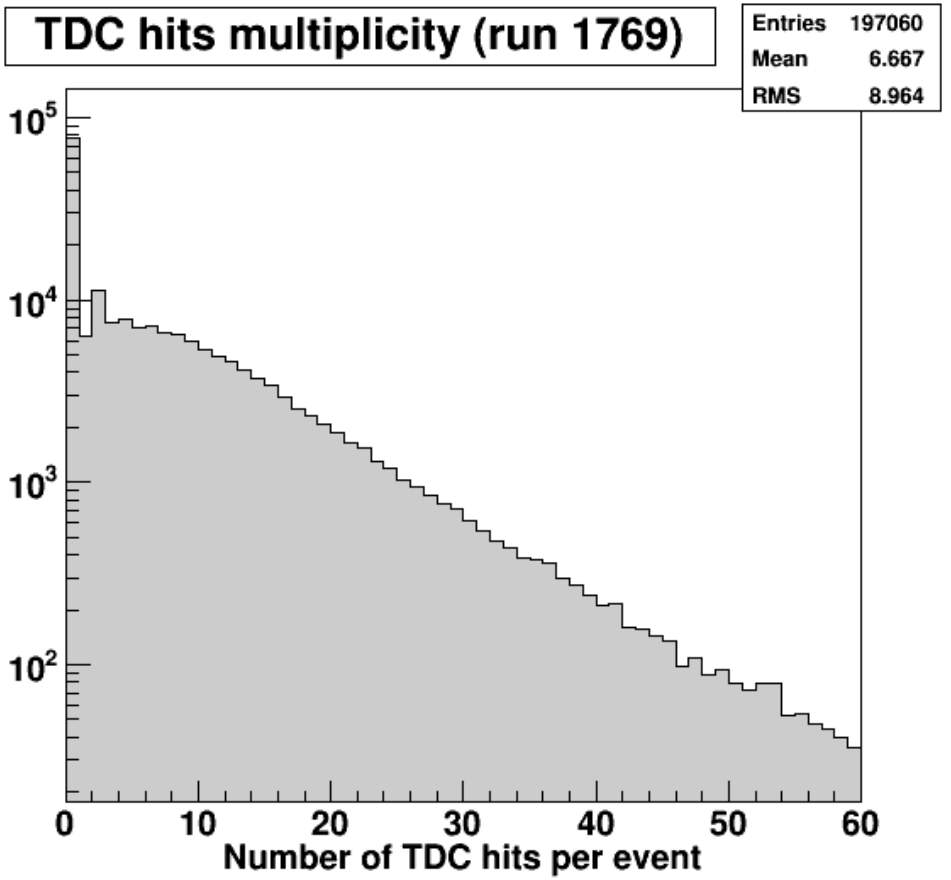
NORTH ← → SOUTH



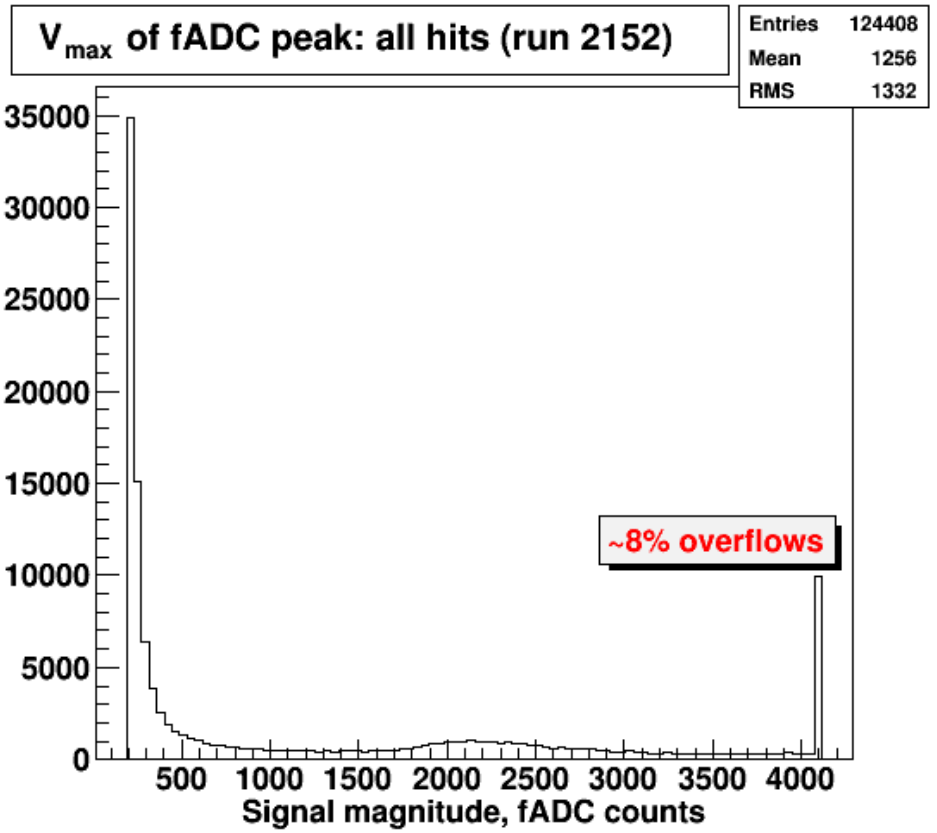
- Rate scales with current/radiator: 120 kHz * (3x10-4/2x10-5) * (150 nA / 200 nA) = 1.35 MHz
- No obvious deterioration of TOF performance at high rate but more detailed study is needed

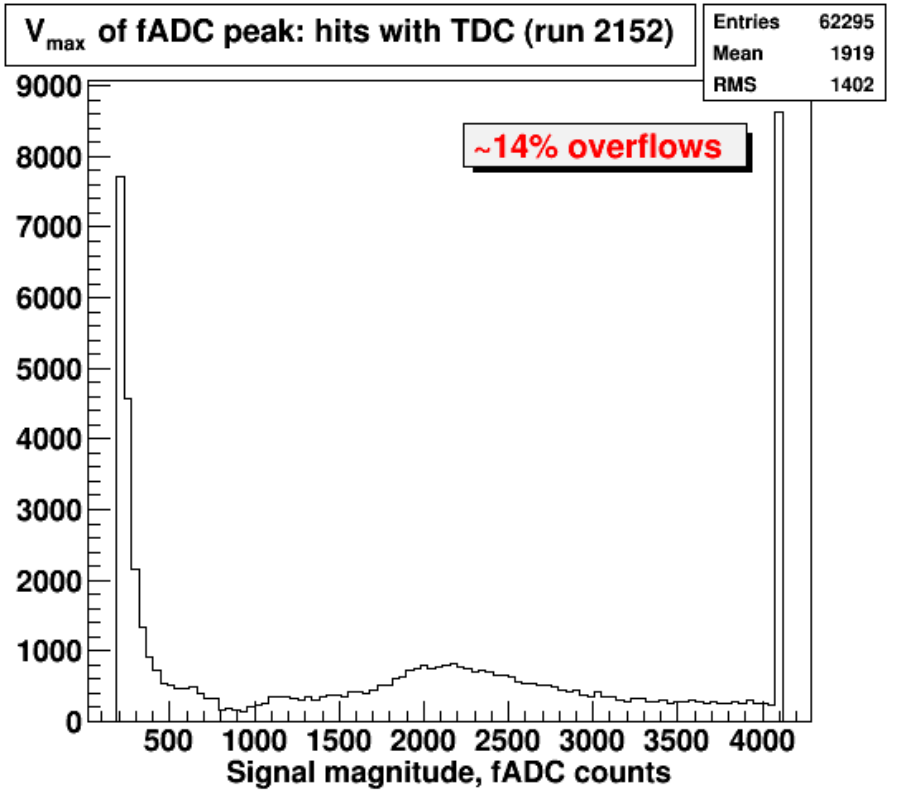
Hits Multiplicity: Run 1769
50 nA, 2x10^{-5} radiator, fcal_m8 trigger



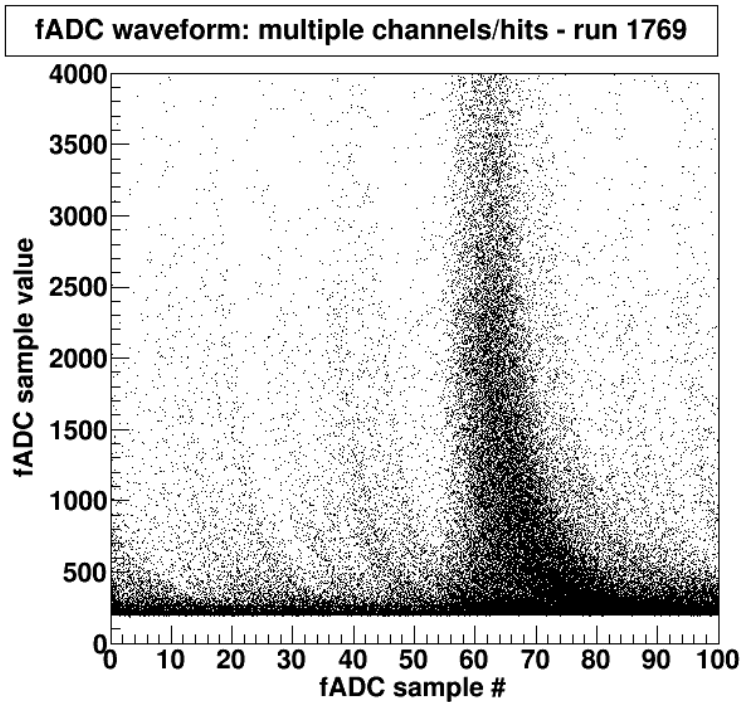


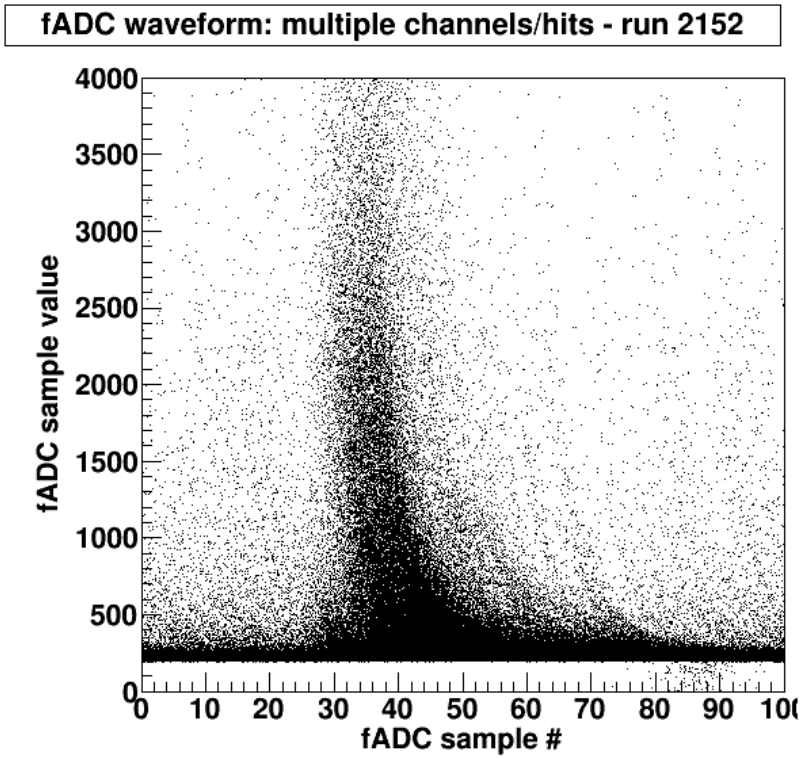
Magnitude of fADC peaks

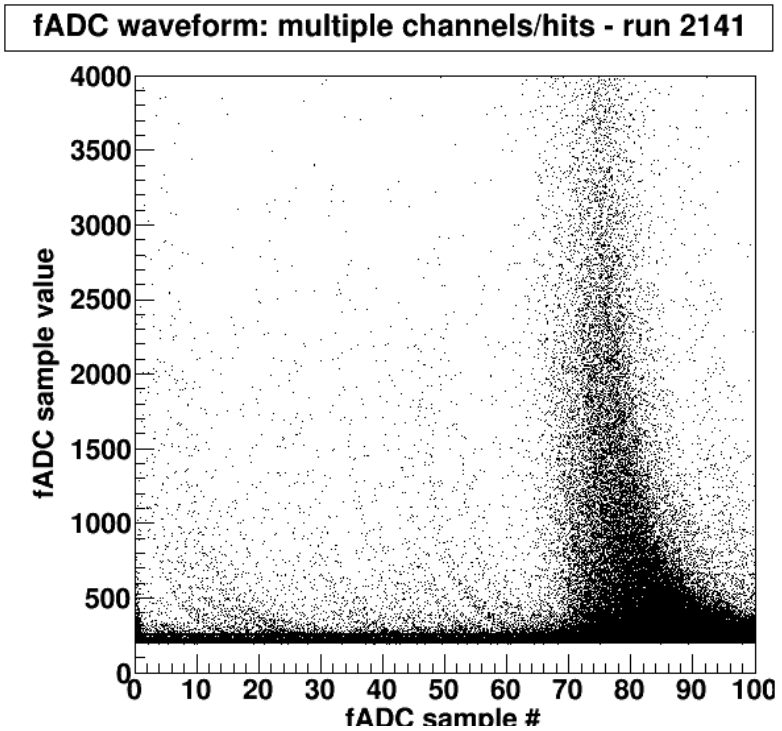


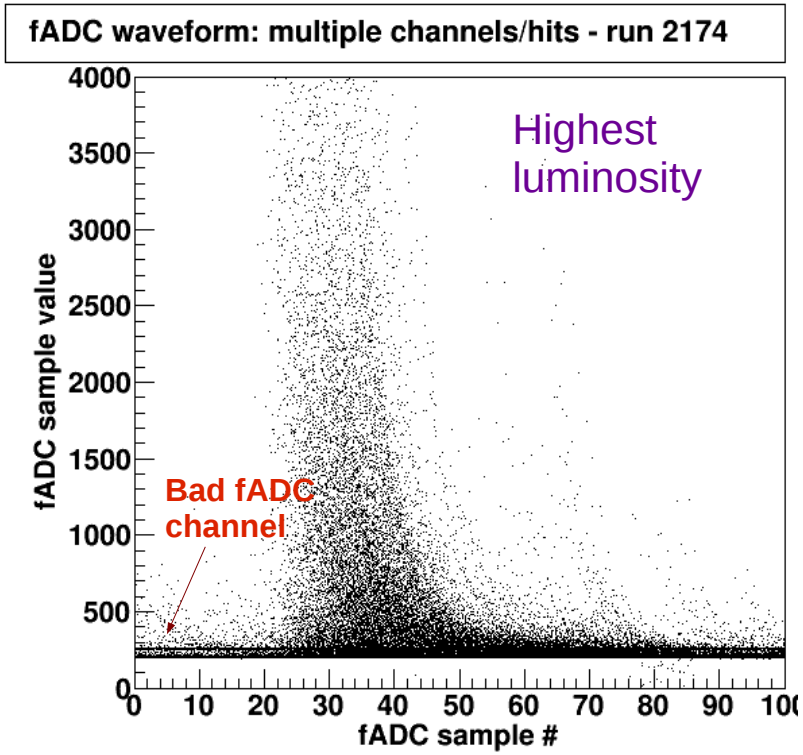


- 8% of all fADC hits and 14% of hits with TDC pair overflow fADC range
- Shoould we switch FADC250 from 1V to 2V range?









Waveform of fADC pulses

- All hits combined
- Integration may be affected if close to the edge
- Yesterday, one channel's baseline jumped from 200 to 260 without any clear reason

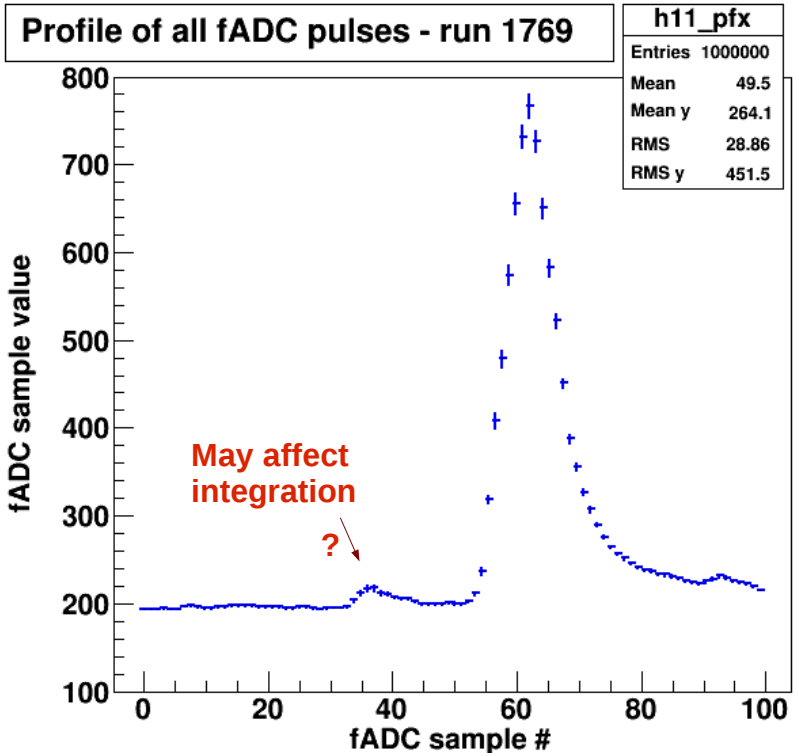
“Average” (profile) fADC pulse

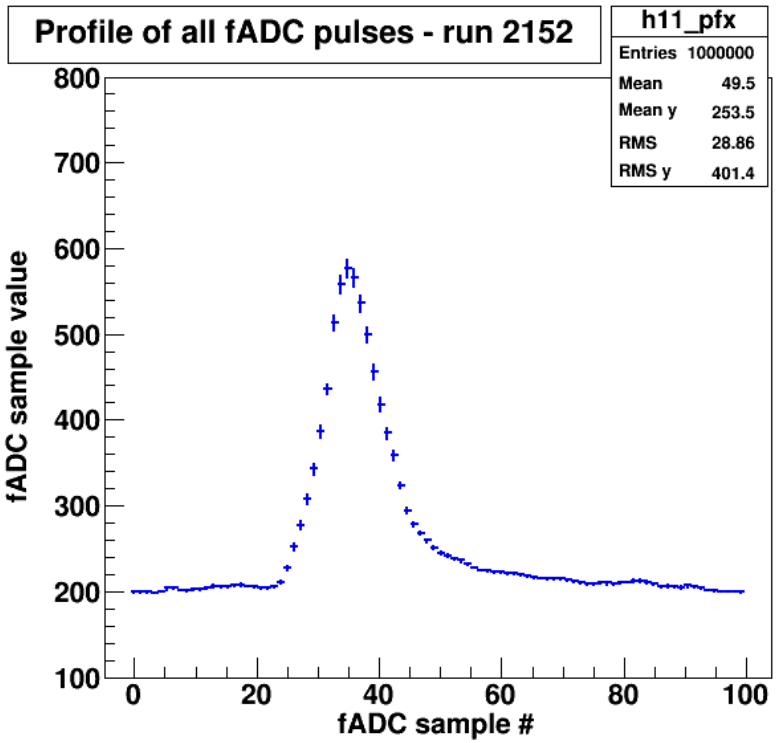
- The nature of “prequel” to the signal is unclear; integration of the main pulse may be affected even with NSA=45

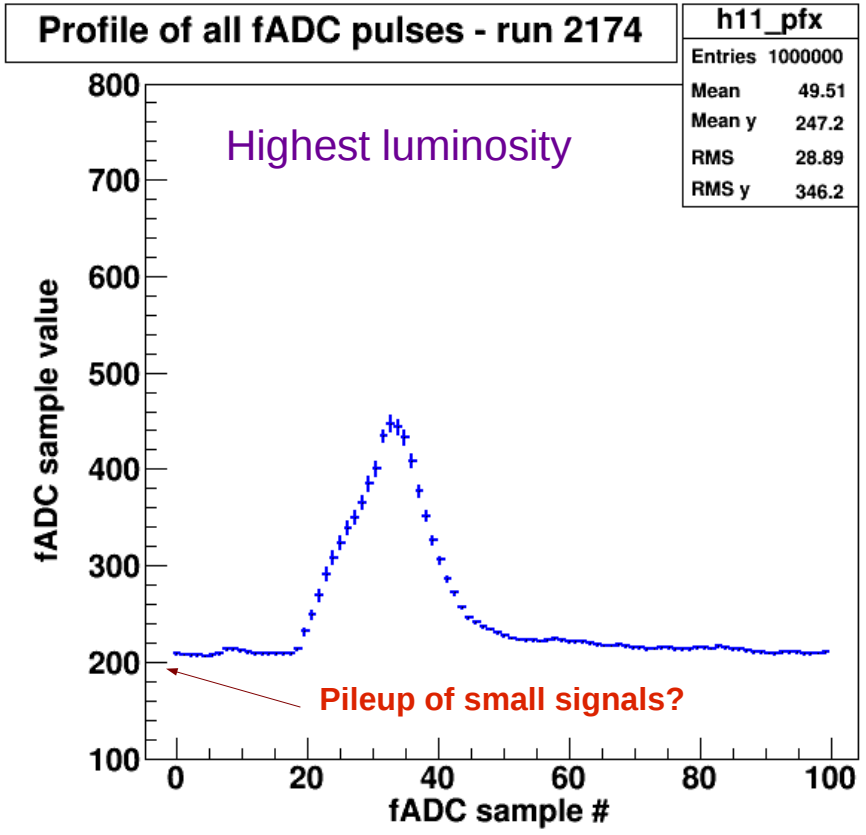
- Can smaller average pulse in 2152 (vs 1769) be explained by fcal_bcal.conf vs fcal.conf?

- In the highest lum. 2174, average*) pulse is higher than baseline (which is still at 200)

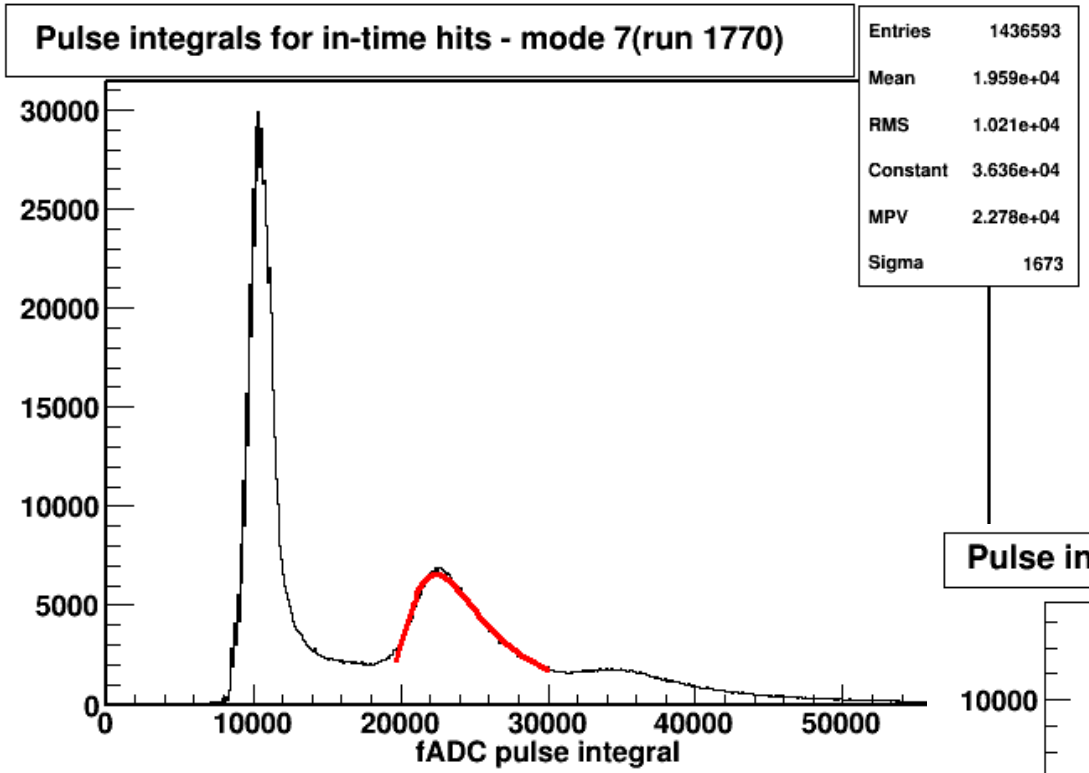
*) bad channel excluded

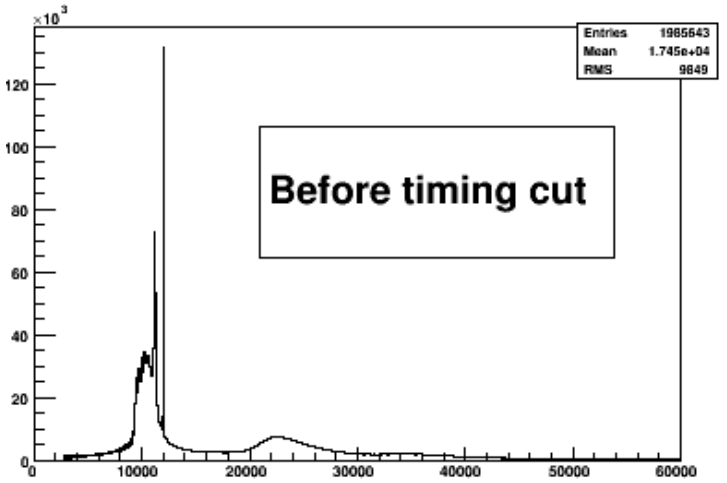


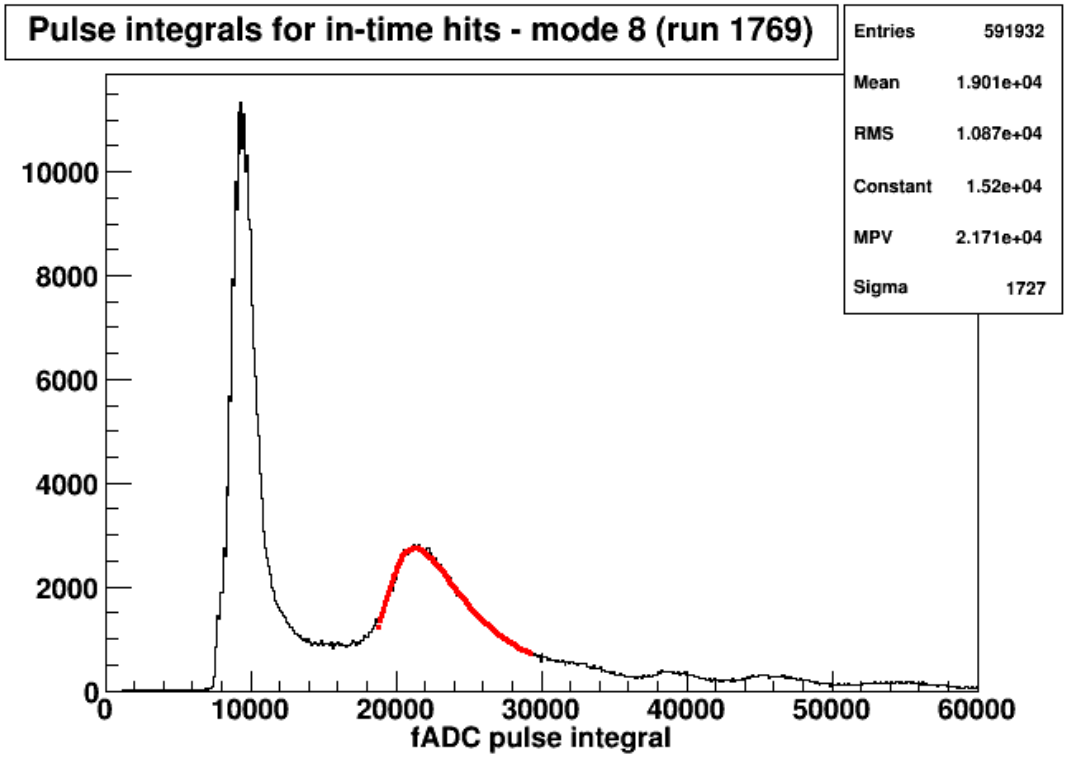




fADC pulse integrals

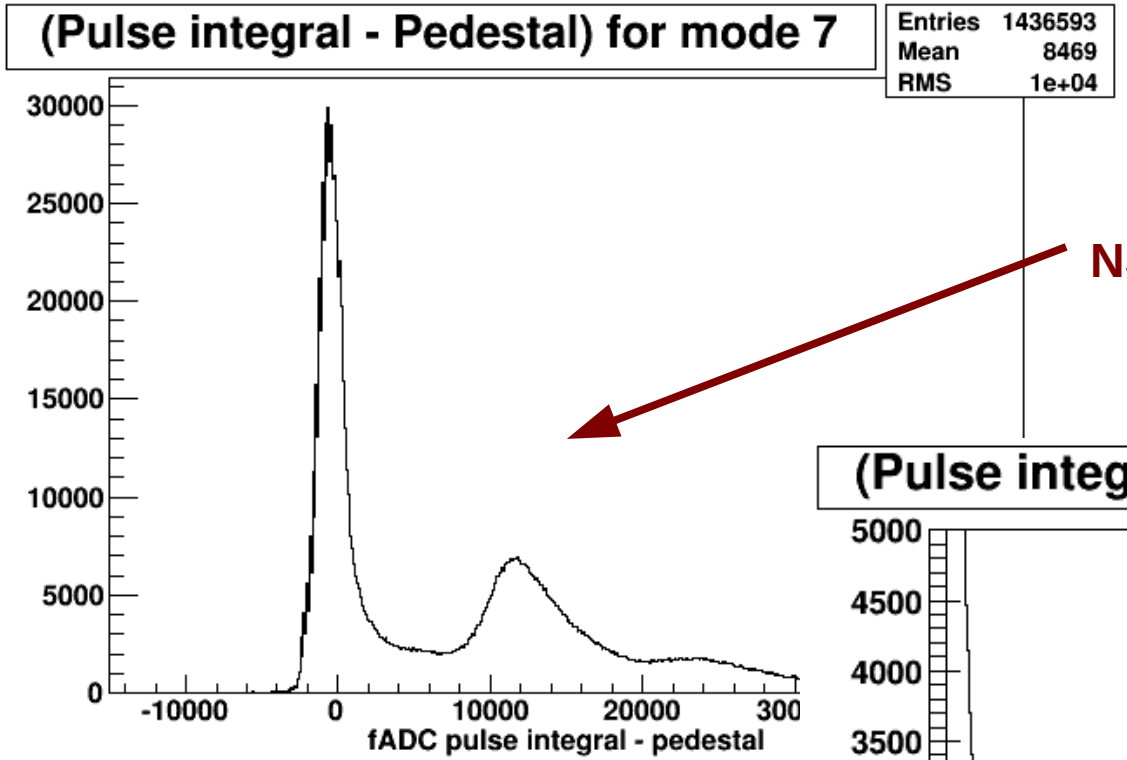




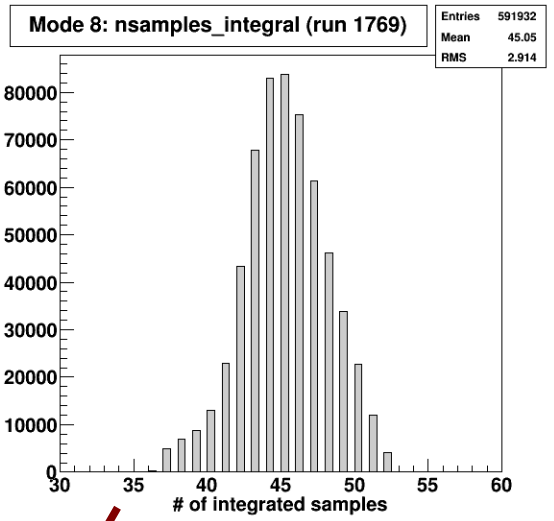


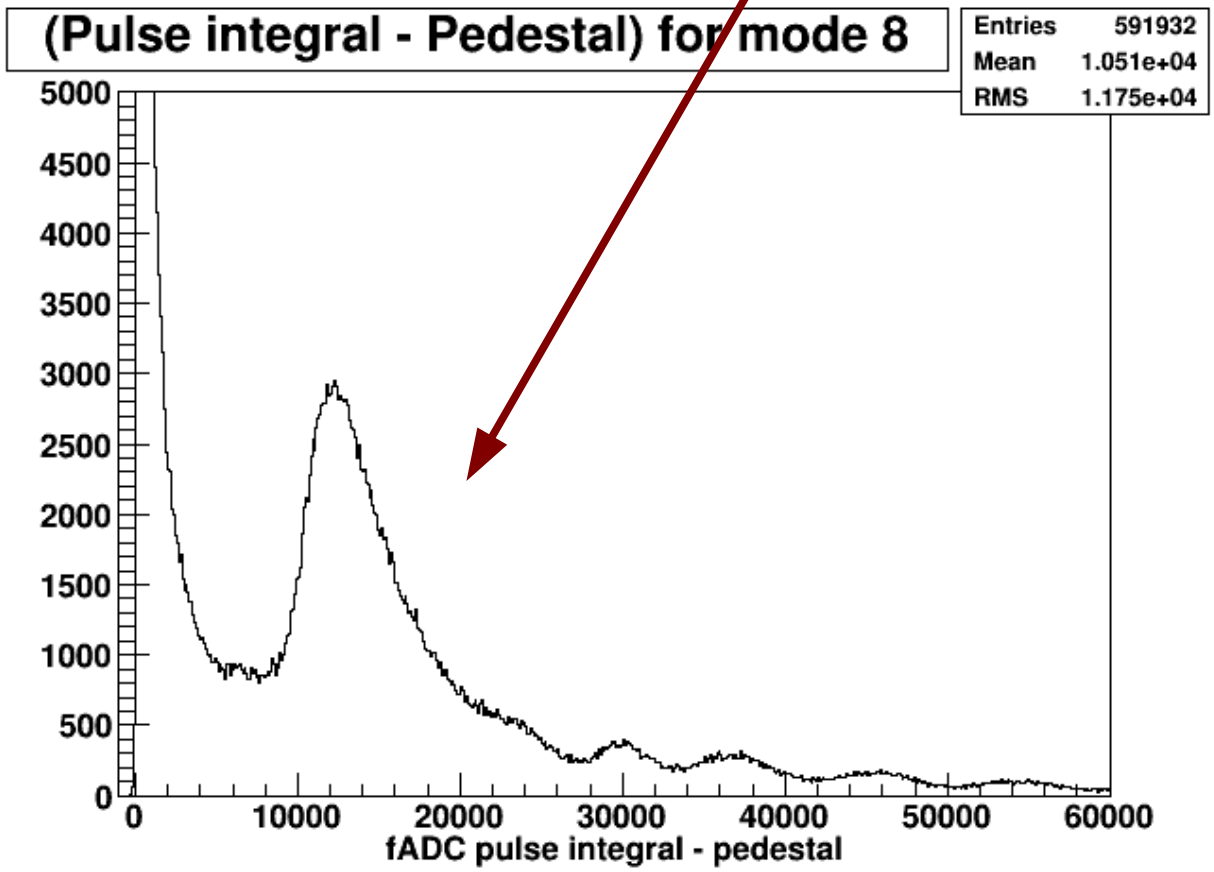
Firmware integration (mode 7) and JANA integration (mode 8) result In similar distribution of fADC pulse integrals

fADC pulse integrals – pedestal subtraction



fixed
NSA+NSB

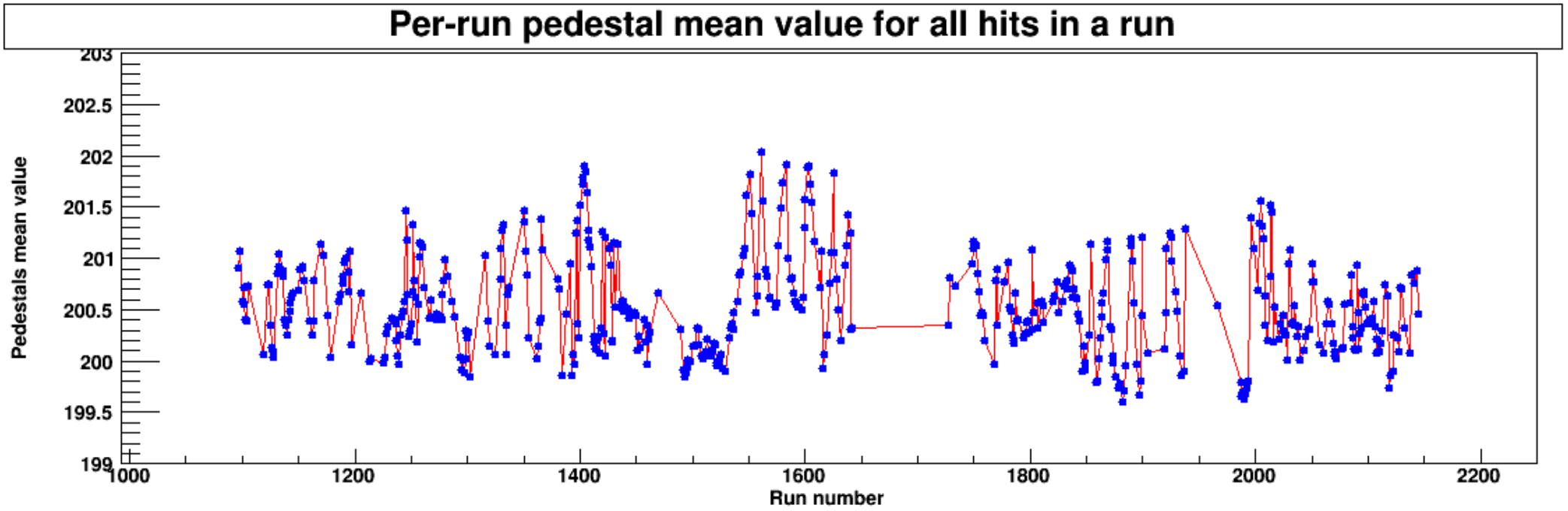


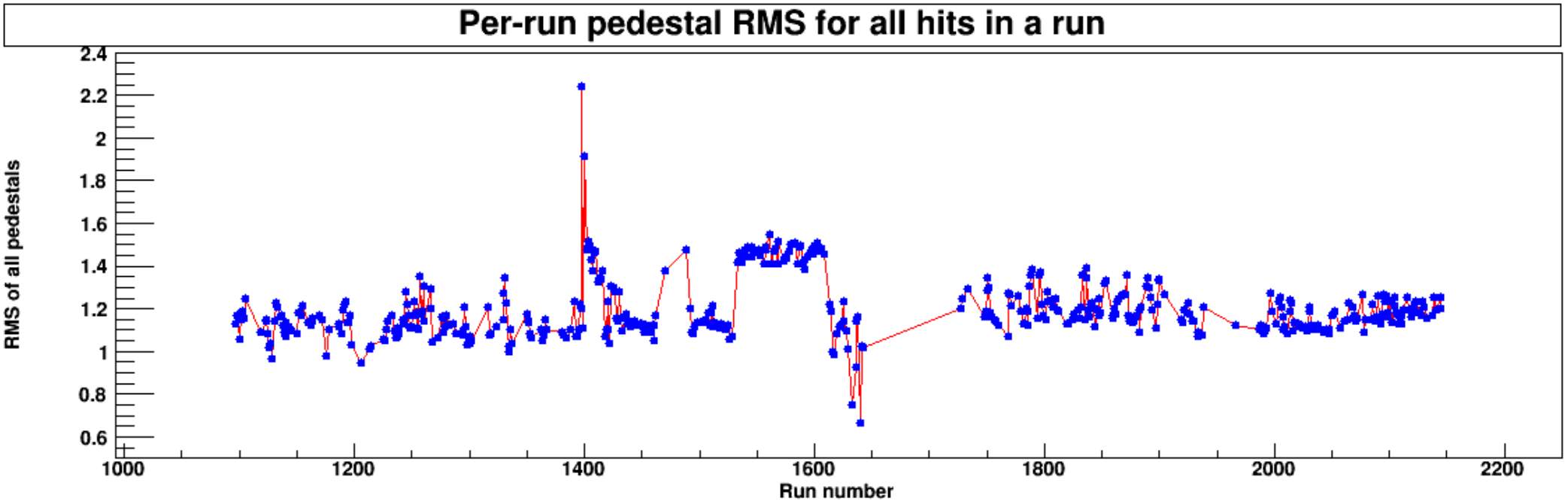


- Mode 7 pedestal subtraction deviates from mode 8 for small signals

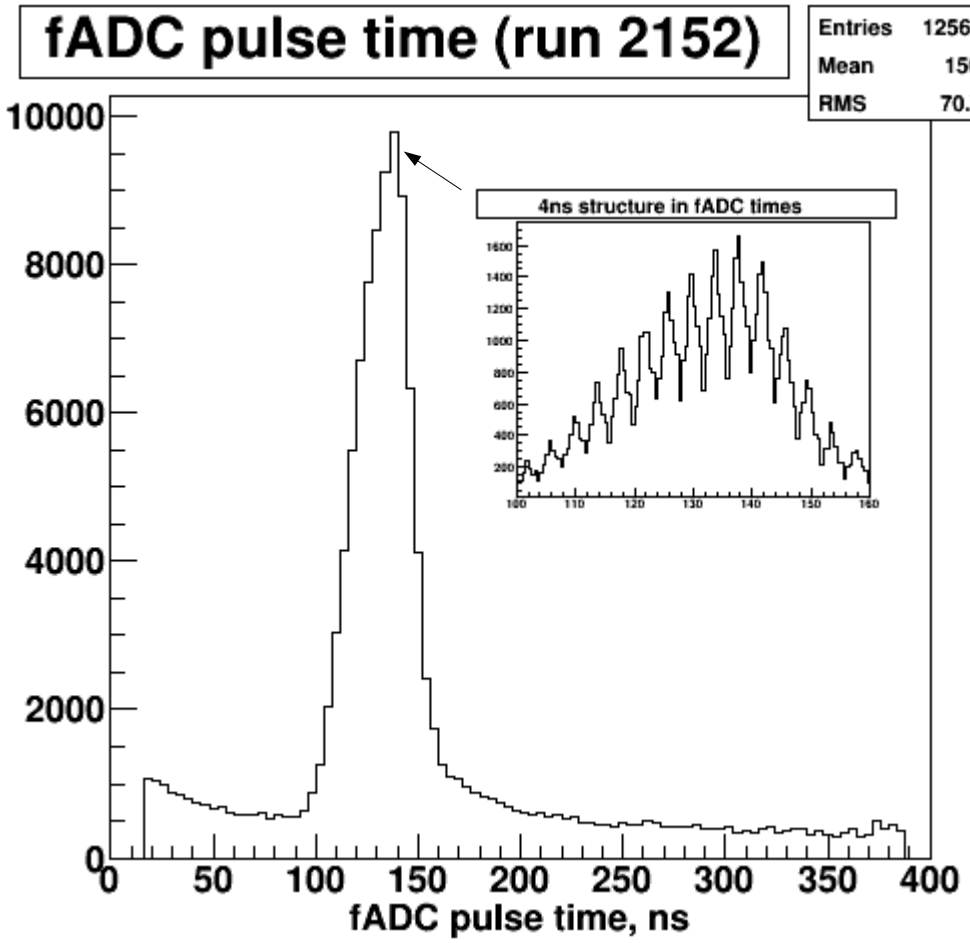
- This creates a problem for time walk corrections in mode 7

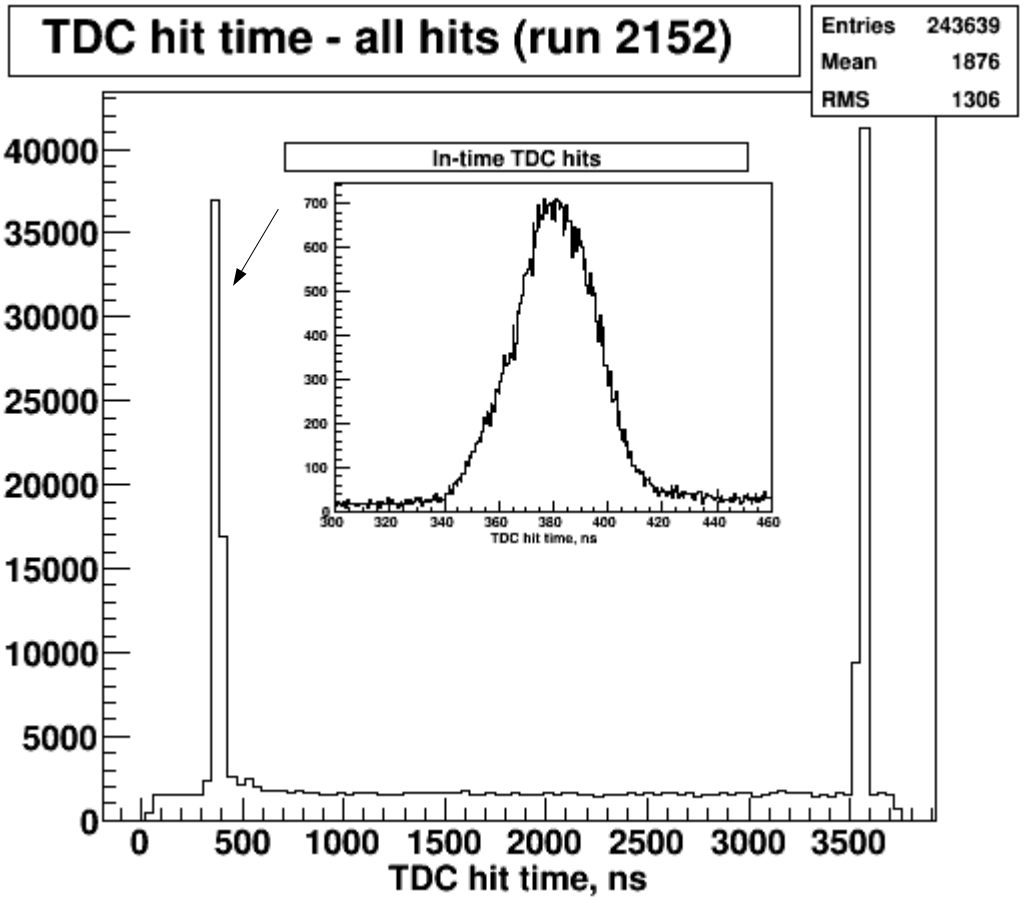
FADC pedestals – one month interval





TOF fADC250 and CAEN TDC timing

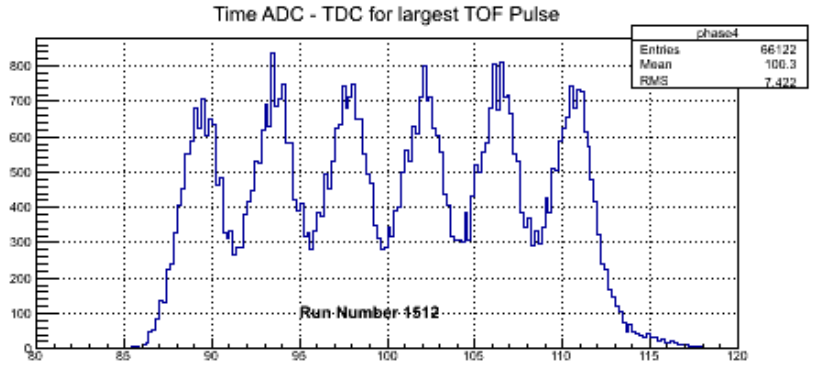


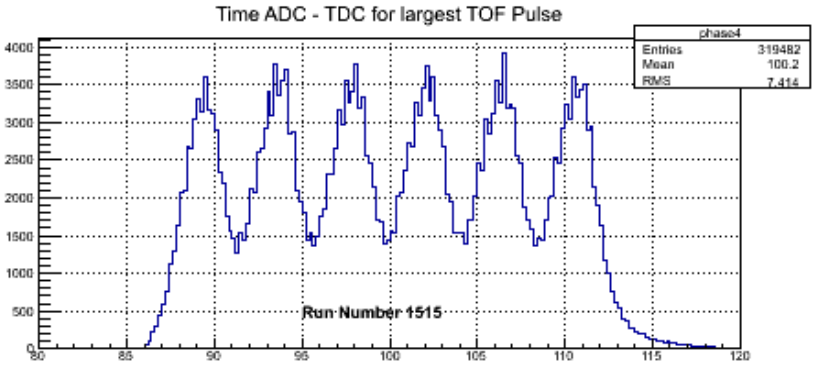


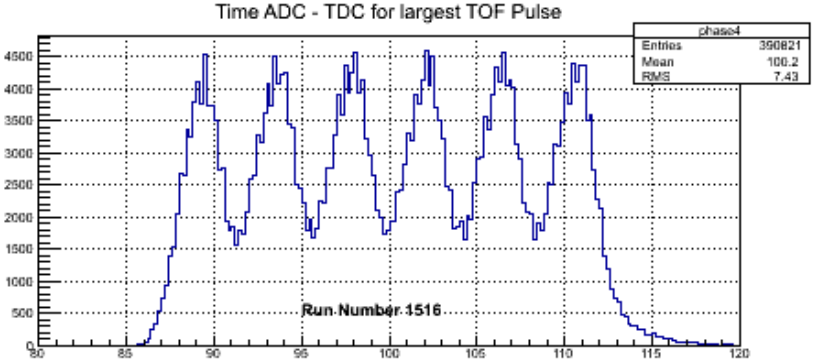
- About 80 ns spread of both fADC and TDC times relative to the trigger
- FADC firmware algorithm with 62.5 ps step nevertheless results in 4 ns structure

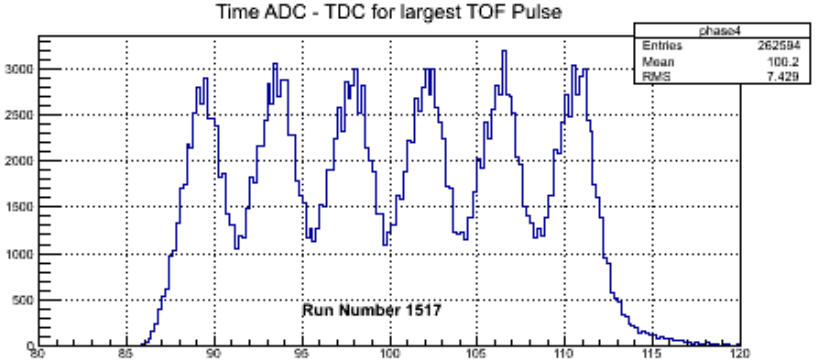
TOF TDC clock phase with trigger

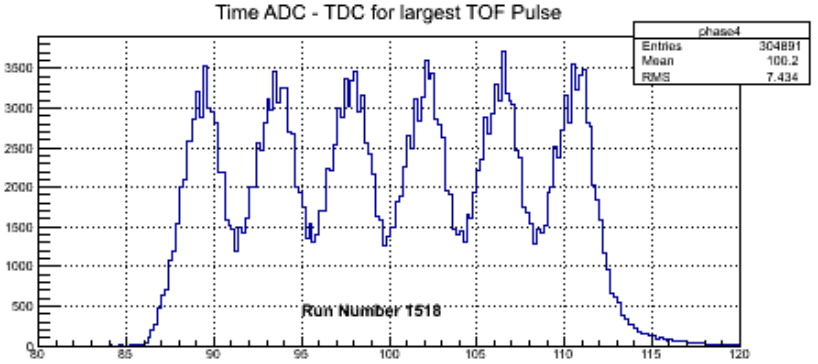
Lognumber 3309602. Submitted by zihlmann on Sun, 11/30/2014 - 14:45.

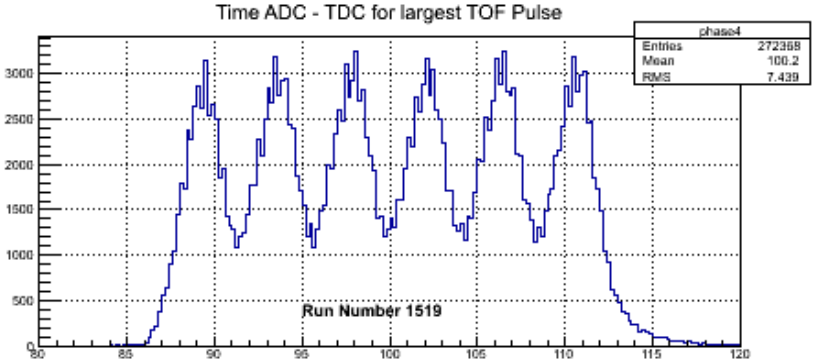








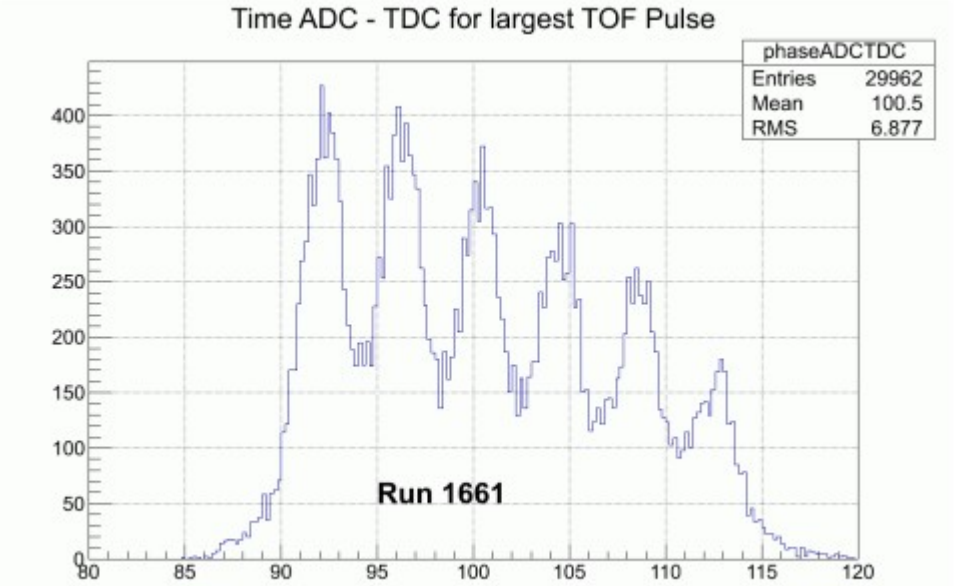




TOF TDC clock phase with trigger

Lognumber 3309602. Submitted by zihlmann on Sun, 11/30/2014 - 14:45.

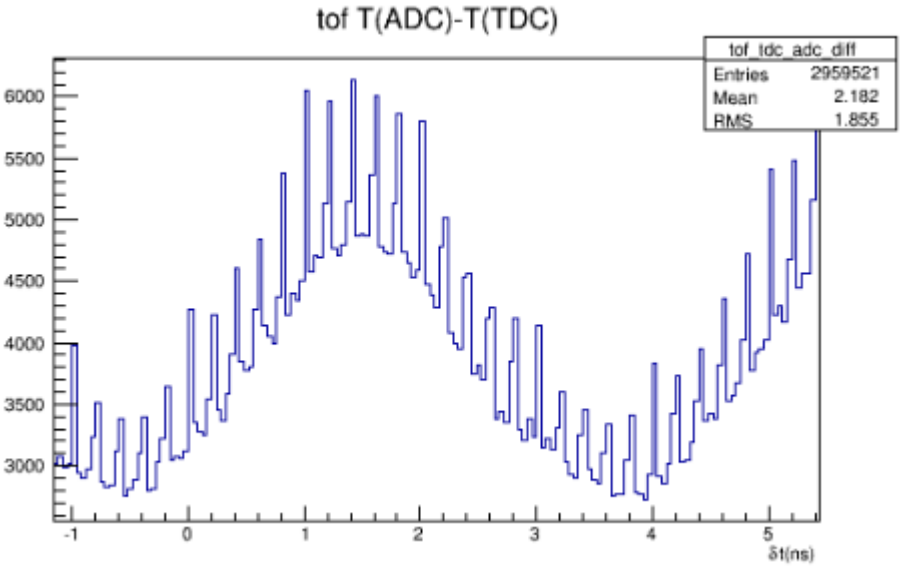
- In high luminosity run:
  - the phase shifted by a few ns;
  - a slope appeared due to dead time



time difference between ADC and TDC for TOF from Run 1515

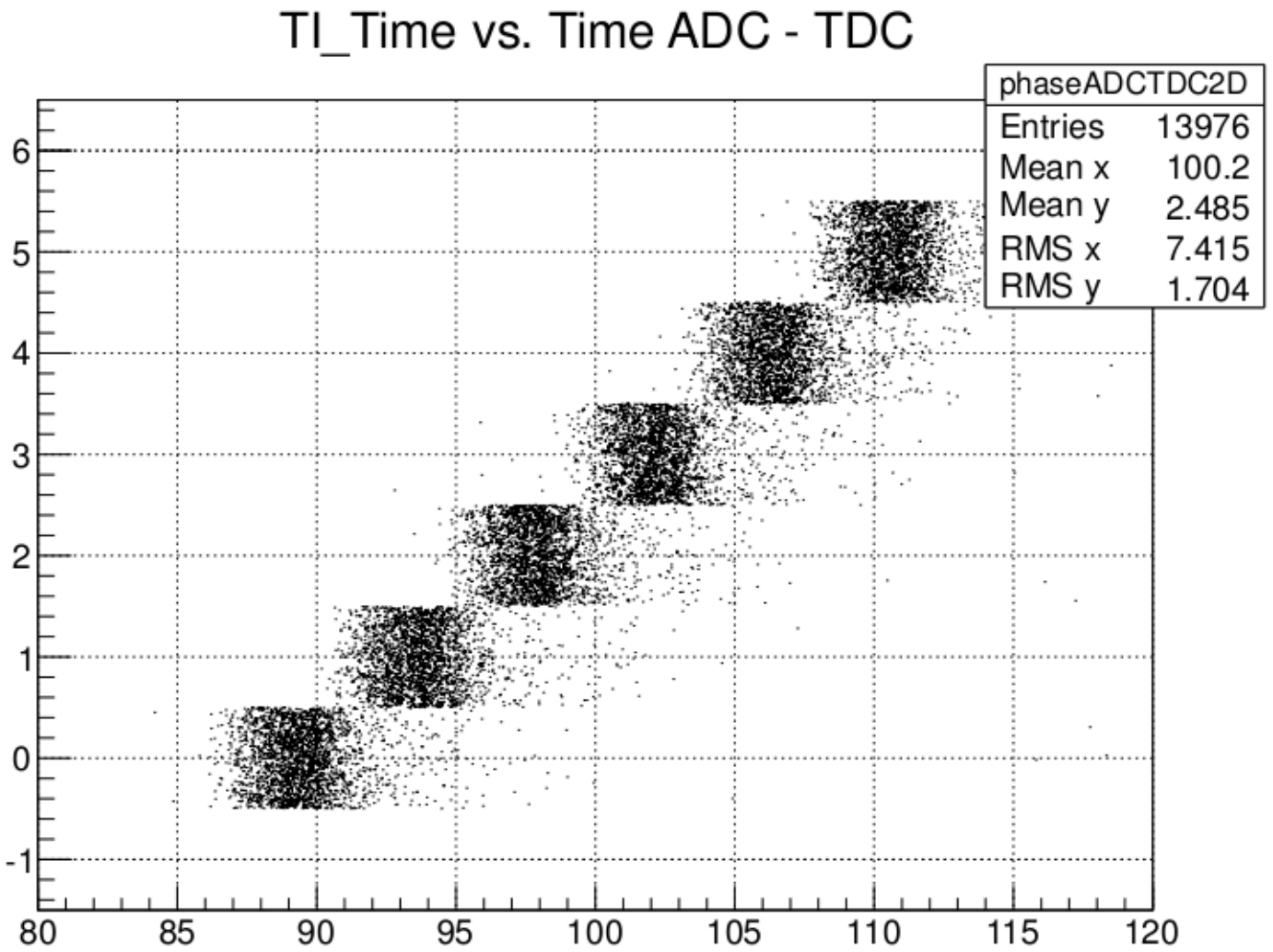
Lognumber 3310104. Submitted by staylor on Wed, 12/03/2014 - 10:46.

- a peculiar substructure with a period of ~200 ps

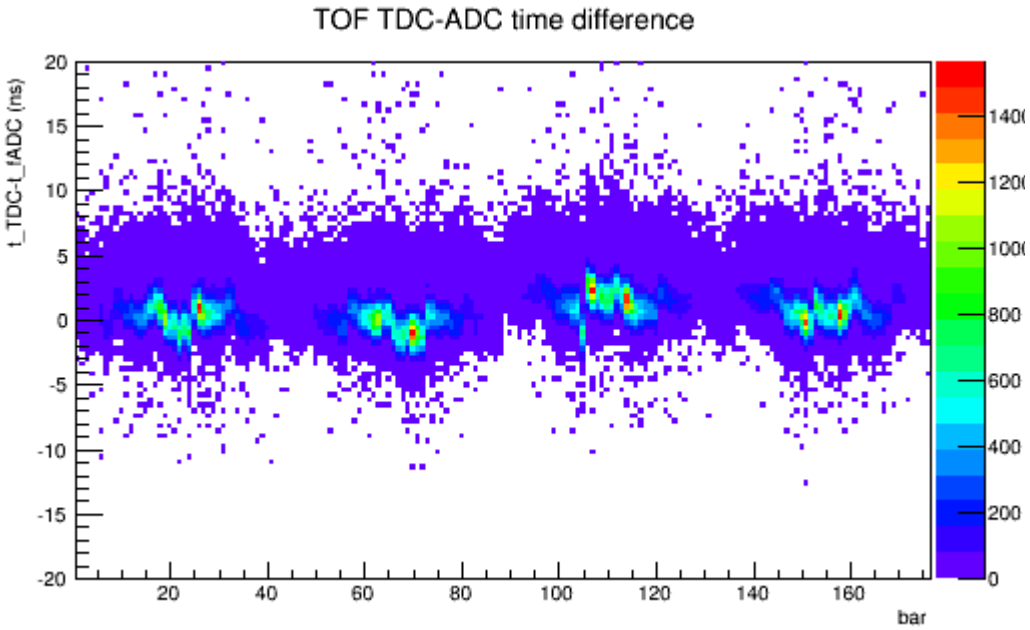
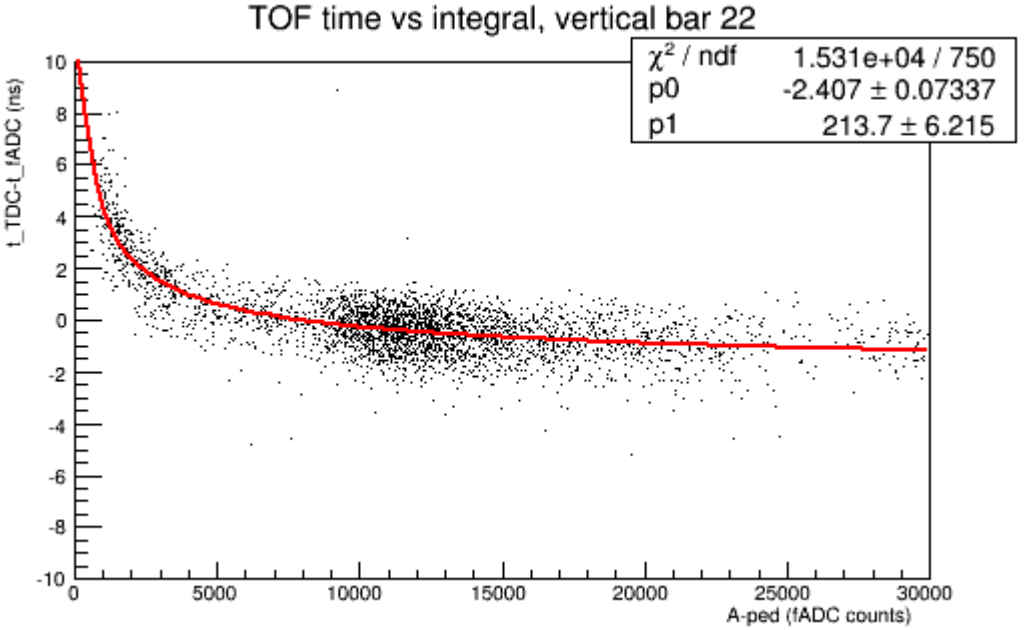
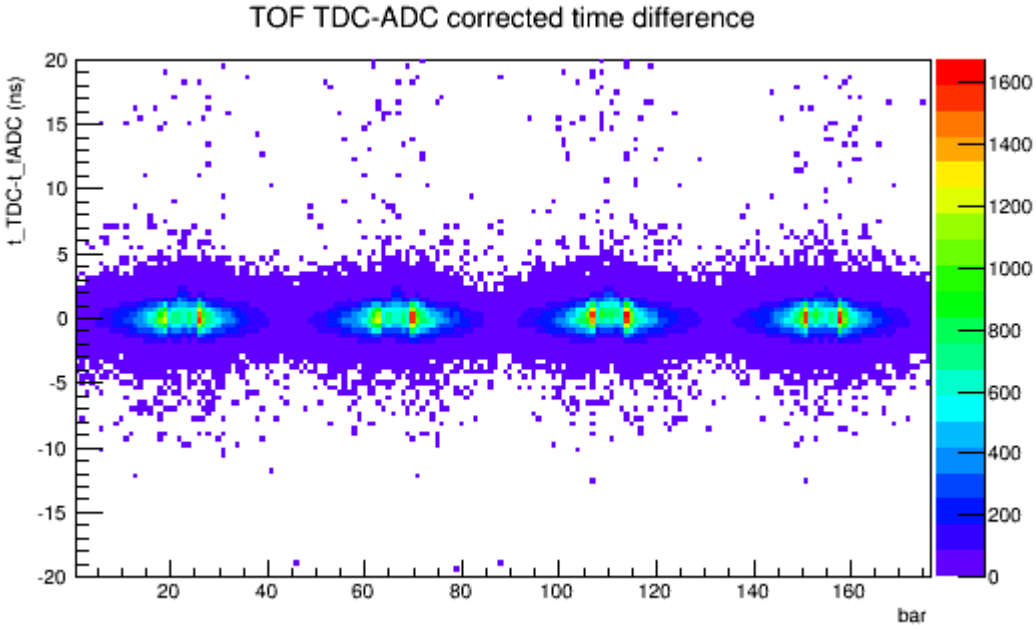
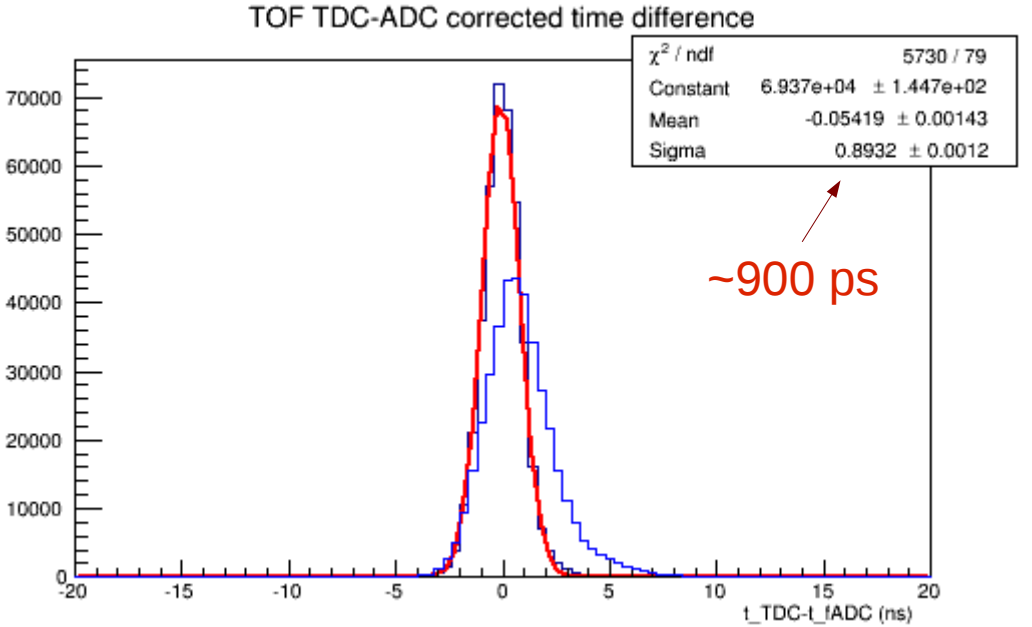


Time correlation with TI timestamp

Lognumber 3310913. Submitted by marki on Fri, 12/05/2014 - 11:57.



- Phase correction may require per-run calibration

timewalk correction for TOF

Lognumber 3311522. Submitted by staylor on Sun, 12/07/2014 - 14:11.