Trigger meeting notes:

17 April 09: C. Cuevas, A. Gupta, B. Raydo, F. Barbosa; M. Taylor; A. Somov, J. Wilson, D. Abbott

10 April 09: No meeting

3 April 09: C. Cuevas, A. Gupta, B. Raydo, F. Barbosa; M. Taylor; A. Somov, E. Jastrzembski; J. Wilson

27 March 09: C. Cuevas, A. Gupta, B. Raydo, F. Barbosa; M. Taylor; A. Somov, E. Jastrzembski; J. Wilson

Updated prototype board status table:--3 April 2009

Quantity	Description	Location	STATUS
5	**10bit FADC250**	**EEL109/DAQ Lab**	**All boards are in use.. Source Synchronous Transfer (SST) Firmware in final test**
1	**10bit FADC250**	**EEL109**	**Received from ORNL**
1	**10bit FADC250**	**EEL109/DAQ Lab**	**Experiment testing successful! Returned to DAQ Lab**
1	**10bit FADC250**	**EEL109**	**Needs repair; Clock Issues**
1	**12bit FADC250**	**EEL109**	**Received 12Mar09 SNR tests virtually complete Ben**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** **F**ront **P**ane**l** – **S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Initial functional testing continues. 2nd board to be tested week of 30March Functional testing needs to be complete by 10 April**

0. Trigger/Clock/Sync – TI/TD

17 April 2009

C code from Sebouh is used when using the Motorola SBC to interface to the TI and CTP. Ben has slightly modified the code but progress continues. The present design of the TI relies on a microcontroller from Atmel to manage the I^2C data from the switch slots. (CTP and SD respectively).

CTP readback is complete, and Ben is integrating the control code with his MSVisual Studio and Root GUI.

SD board is ready to test with control registers by close of business today, 17April09. Abhishek has been working on the Altera code for controlling the required registers on the SD board. These control registers are not required for the two crate test, but will need to be thoroughly tested to complete the prototype design phase.

3 April 2009

Sebouh continues with testing his GUI and I^2C interface for the CTP. He uses the Wiener VME to USB controller and has completed C code to control the CTP register functions, and the data is displayed on his GUI that has been developed with MicroSoft Visual Studio.

Sebouh has delivered his draft report, and his documentation is very complete. He will need some time to test his control interface with the SD board, and when there is more time he will integrate the Virtex 5 monitoring features. (Temperatures, voltages, etc)

27 March 2009

→Sebouh can proceed with further development using the VXS test crate by adding wires to the CTP boards so that they receive the I^2C signals from PayloadPort 10. The 20 slot backplanes are occupied with SD testing, so having the alternative method to continue the CTP interface control testing will be useful for a few weeks.

→I^2C control and monitoring for the SD board will begin by the week of 6 April. Abhishek and Sebouh will have to work together to ratify their respective firmware so that control of the SD board is robust and ready for testing in the 20 slot backplane crates

1. FIRMWARE TESTING

17 April 2009

Significant progress has been completed with the VME-SST firmware. Several (4) FADC250 boards have been loaded with the new SST firmware and testing continues in the lab. Token passing with multiple boards has been tested, and the token passing scheme appears to work. We can use wire jumpers on the backplane (P2) to test the boards in the two crates in case the SD board token passing logic is not ready.

3 April 2009

Firmware development for the VME SST mode is complete and at least two of the FADC250 have been loaded with this new firmware. Ed reports that there are a few more details to work through, and testing with the token passing, interrupt mode and polling mode plus readout of multiple modules is a work in progress.

Ben has started testing the 12 bit FADC with the new SST mode and has worked with Ed to devise a way to inject signals during the SST bus cycle. Ben has gathered SNR data with the 12 bit module, and is prepared to show results at the next meeting.

27 March 2009

→Ed reports that the SST mode is working on the FADC250 module and he is testing the board with the token passing scheme. The Retry* signal will need to be wired on the FADC250 Altera Fpga to satisfy the SST block transfer features.

→By the week of 6 April, the new SST firmware can be copied to the FADC250 boards and testing can begin with the boards in the 20 slot VXS crates. There are several tests to complete by using the SD module as the token pass 'hub', including the logic to control the BUSY signals from each FADC250 modules.

2. *SUB-SYSTEM PROCESSOR (SSP)*

17 April 2009

Altium CAD files presented and the FPGA have been added to the schematic successfully. The hierarchy tools for the front end fiber optic receiver circuits has been used, and there are several errors to correct before all of the components are correctly loaded in the circuit board 'project'. Many schematic circuits need to be defined yet, but progress is detectable.

3 April 2009

All three FPGA have been added to the schematic and CAD plots were presented that show the overall hierarchy layout plan. Two Virtex 5 FX70T will manage the front end fiber optic transceivers, and the Virtex 5 LX30T will handle the VME interface and the trigger data streams from each FX70T. Provisions for controlling the FX70T devices will use a high speed control bus, and there are many components still to be added to the schematic.

The FPGA signal manager and hierarchy symbols are a very powerful feature of the Altium CAD program and it will take some time to thoroughly understand all of the critical steps. I plan to move from the schematic capture work, to an initial board layout by next meeting.

27 March 2009

The V5LX30T FPGA has been added to the schematic and the VME interface and local control bus will be managed by this chip. The MGT on the LX30T will be connected to P0 and ultimately to the GTP. Two V5FX70T FPGA will be added to the schematic to interface to the eight Fiber Optic transceivers. Plenty of schematic work to do, but I am using this design as my full fledged tutorial with the new Altium CAE/CAD tools. So far so good, albeit my slow progress.

3. CUSTOMERS

17 April 2009

→Hall A has presented a proposal to use a prototype FADC250 module for their Moller experiment scheduled for September '09. Hai has completed the firmware and has simulated the code. Ed will need to add the new features for the Altera FPGA and a few software 'library' changes need to be added to control these new features. Testing the new firmware for the Moller application will be a lower priority than the two crate trigger testing.

→Brad Sawatsky presented data that was collected by an FADC250 prototype module on a recent Hall A experiment (Big Bite Cernkov detector). The results were encouraging and he seemed pleased with the results. There was a question about optimizing the 'window' and look back time, but they were able to write the necessary analysis programs to use the data.

→The eight channel 12bit module will be sent back to the IU-FCAL group before the end of April. Ben has collected SNR data and if there is time, it would be nice to run a test to compare the 12bit FADC250 to the LeCroy QDC module. Ben has recorded the results from the comparison of the 10bit FADC250 Vs the LeCroy QDC, so the results from the 12 bit module would be interesting.

3 April 2009

Brad Sawatzky has been invited to present initial data that was collected with a 10 bit FADC-250 module on a recent Hall A experiment. He is scheduled to talk at the 17April meeting.

Ben has been testing the 12 bit FADC250 and will present SNR results at the 17April meeting. We can return the 12 bit module to the IU group before the end of the month.

Hai has completed the firmware for the Moller Daq experiment that has been proposed by Eugene Chudakov and Bob Michaels. Presumably the firmware has been simulated, but will need further testing in the lab using signal generators for the front end signal testing.

27 March 2009

Data from the latest Hall A experiment will be requested by Chris for a brief presentation by the Hall A Users. I believe they were successful, and it would be interesting to hear about the results.

There is a request to use a single FADC250 as an upgrade to the Moller Daq in Hall A in about 4 months. Hai is presently working on the changes to the firmware (V4FX20) that will be necessary for the experiment proposal. The experiment does not require the use of the VXS

trigger data transmission and testing can begin after the work for the trigger test stand is complete.

4 "B" Switch - Signal Distribution Module (SD)

17 April 2009

→Abhishek presented waveform photos from the oscilloscope for a variety of payload ports and signals. The clock waveforms and pulse shapes for the SYNC and TRIG signals appear to be the correct levels and there were a few pulse shapes that did not look consistent. The scales on the O'scope need to be the same, and some of the pulse shape attributes, (i.e. risetime, fall time) were attributed to the high speed differential O'scope probe connections. Good news is the signals appear without excessive ringing, or other anomalies.

→The control code for the SD Altera device is progressing. Controlling the select lines to choose which payload slots receive a specific clock, and writing the mask register for the BUSY and TOKEN IN/OUT signals will need to be verified with Sebouh's I^2C firmware. Implementation and functional testing continue.

3 April 2009

→Plenty of testing with the initial SD module and it is critical to verify the operation of the 2nd SD module. The two crate trigger module test will require that both SD modules are preconfigured so that on power-up they fan out the 250MHz clock to all payload slots. The trigger and sync signals will also be fanned out to all slots.

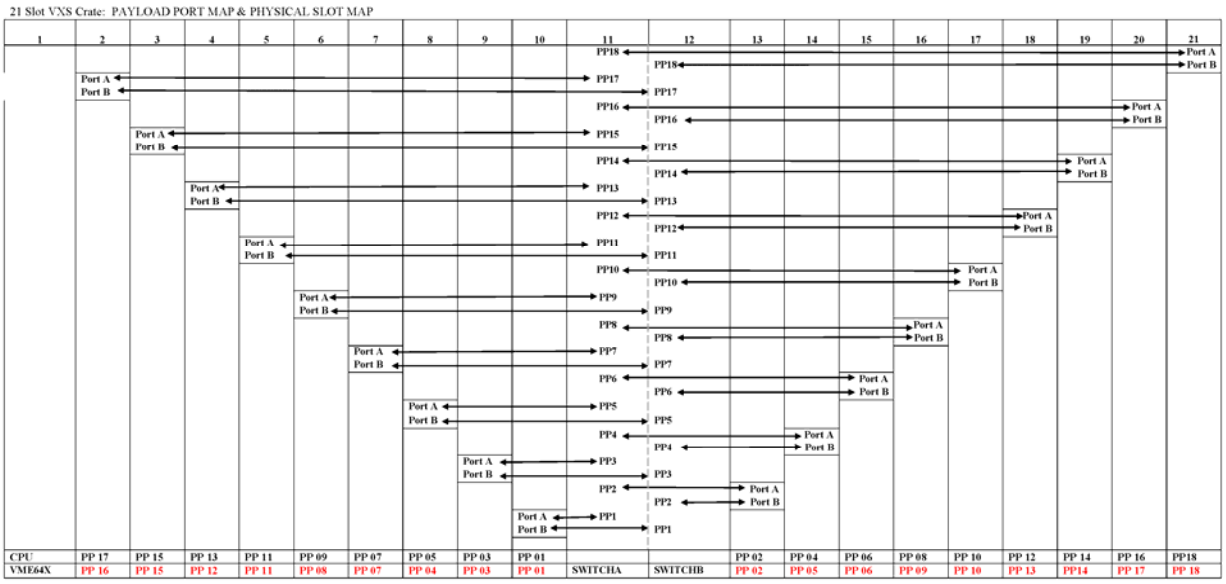
→RECORD all test measurements for both SD modules and document these test measurements in a concise table that shows the design meets or exceeds the specifications. There are a number of tests that still need to be performed, but we need the SD modules to continue the two crate trigger module testing.

→Work with Sebouh to include the control and monitoring features of the SD module using his GUI and software work. Additional SD firmware work remains for complete testing of the token passing and BUSY signaling and control.

27 March 2009

→Abhishek and Mark's measurements of the clock jitter as it is received on the FADC250 were presented and the results are very promising. Initial results for the jitter of a received 250MHz clock is ~3ps and the histogram showed a peculiar 'picket fence' display.

→The Wiener (Hartmann) backplane is indeed different than what was specified and apparently they were able to save 8 layers on their backplane design by adopting a different PayloadPort map. See the drawing below: (pdf file so you can zoom)



We will continue to test with both VXS backplanes and record any differences. The PayloaPort mapping from Wiener is their creation and effectively makes the design a sole-source. Several companies sell 20 slot VXS backplanes using the 'Elma' port mapping, and we have designed the SD and TI boards to follow. The Wiener backplane is not unusable, but it adds a bit of confusion to an already crowded room full of slots, port maps, pins, lanes, switch slots, etc.

5. System Diagrams & Test Stand Activities

17 April 2009

Nothing new to report, and other items have become a higher priority, but Jeff mentioned that the initial routing to a single FPGA for all sixteen ADC will work on four routing layers. The cost analysis of using a single FPGA will need to be performed for the Rev-1 design. Virtex 6 anybody?

3 April 2009

A few discussion points about the single FPGA idea for FADC-250 Rev-1 were exchanged and a cost analysis will need to be completed soon.

Alex discusses the idea of loading the FADC250 front end FPGA with data so that the entire trigger system 'chain' can be tested. There are provisions to load the FPGA with new firmware, and we will need to create a set of requirements for this type of overall system test mode. Other types of input to the trigger system will need to be included in the requirement list, including exactly what signals need to have scalers. (i.e. Scalers==Counters, Trigger counter, Hit_Bit counters for 'hot' channels, CTP, SD, SSP). All the boards in the system have FPGA and implementing counters on important channels for diagnostic purposes will be important. How often these counters are readout will need to be defined also.

27 March 2009

→Jeff presented a preliminary route of the proposed 'single Fpga' idea for Rev-1 of the FADC250 board. There will be iterations, and there will be another Fpga for the VME interface and local control bus. The Gigabit transceivers were not routed to P0, but the position of the

single FPGA is planned to accommodate the lanes needed. Plenty of other details remain, and the FADC250 Rev-1 design ideas will continue.

6. Crate Trigger Processor (CTP)

17 April 2009

Hai's test plan continues and the firmware that will be used to capture input pulses to the ADC will be installed and tested next week. The two crate test results are imminent and Hai has generated many hours of successful data transfer between the FADC modules and the CTP. All bit codes have been thoroughly tested, and the SD module has been used to clock and synchronize the boards in the system. The plan is to use four FADC in one crate, and two FADC in the second crate, all clocking from a single TI, synchronized and producing a trigger from a given set of input pulses.

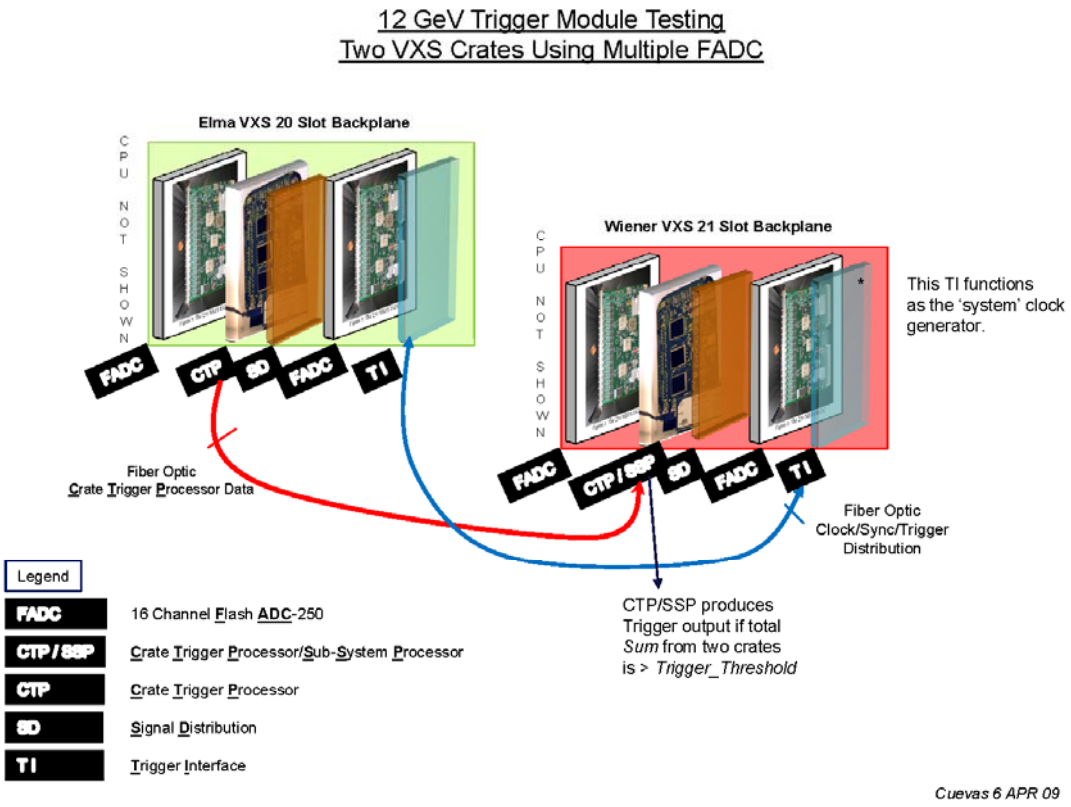
3 April 2009

Hai presented his test plan and showed the progress so far. There are several more steps in the test process and he will be ready to test both CTP with multiple FADC, the SD, and of course the TI modules all running in unison very soon. All testing so far has been very successful with the Gigabit transceivers running at 2.5Gps, for many hours using the longest (150m) fiber cable.

Preparations are under way for the poster information and data needed for the presentation to be given at the IEEE RT conference in Beijing during the second week of May. The block diagram below shows the main components of the two crate trigger module test.

Highlights:

- Two VXS backplanes with all Payload ports available
- Two Crate Trigger Processors (CTP)
- One Crate Trigger Processor operated as a SubSystem Processor
  - CTP/SSP module processes trigger data from FADC250 boards AND trigger data from the 1st crate
- Two Trigger Interface modules (TI)
  - One Trigger Interface operated as the system clock source (Trigger Distribution)
  - Clock; Triggers; Synchronization signals use fiber between crates
- Two Signal Distribution modules (SD)
  - 250MHz clock and other common signals distributed to front end FADC250 modules through the VXS backplane



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27 March 2009

Both CTP are running in the twelve slot VXS crates and Hai has been successful with transporting 'trigger' data from three FADC250 boards to the CTP and then to the 2nd CTP that is operated as an SSP. He has set up a test program and is using Chipscope© to register an error condition. The plan is to continue testing in the twelve slot crates, and then very soon, transfer these boards to the two 20 slot VXS crates and use the SD in each crate to distribute the clocks and common signals to each module in the crates. Once the modules have been configured in the crates, we can distribute signals to various input channels and configure the system to TRIGGER on a particular sum. There are many other test results to record for the IEEE-Real Time Conference poster.

ACTION ITEMS: **Next meeting will be Friday 24 April 2009 → CCF228 @10am**