



THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
JUNE 10, 2013

TITLE: Hall D Solenoid Commissioning

DATE: 2/4/2013

BY: Joshua Ballard

CHK: George Biallas

APP: George Biallas

APP: Timothy Whitlatch

C	Extensive revision to follow on to Rev. B. Verify remaining interlocks. Adds turn-to-turn shorts, ground fault detector qualification and resistance check. Adds possible use of tuned Power Supply with soft ramp to commission Quench Detectors . Adds soft ramp to 140 A and back to zero A.					
B	Extensive revision to include Power Supply Qualification at 15 A, the interlock verification necessary, verification of Ground Fault Detector placement, test for turn-to-turn shorts, calibration of the Quench Detector and leaving final cool-down to LHe temp.	GB	M. Stevens	TW	P. Rossi	5/28/13
A	Incorporated changes recommended by reviews. Updated to reflect actual installation	JTB	TW for GB	TW for GB	TW	2/22/13
REV.	DESCRIPTION	BY	CHK.	APP.	APP.	DATE

Re - Commissioning Goals – Intermediate (140A) Current

1. Re-verify correct operation of all mechanical, cryo, safety interlocks and monitoring/archiving systems beyond those verified under use of Revision B of this Plan.
2. Qualify the Magnet Power Supply (MPS) at **up to 15 A and then at 140 A** in the superconducting state under the Solenoid's inductive load such that improvements such as "tuning" and/or soft ramp profile ramp-up may be measured for their ability to minimize transients, and thus not trip the Quench Detector (QD).
3. Test for turn-to-turn shorts
4. Verify that the Ground Fault Detector (GFD) continues to not trip at the above currents and attempt to lower its sensitivity to less than 180 mV.
5. Demonstrate that the PLC Quench Detectors operate over both current ranges.
6. Adjust the Balance and Sensitivity of Channel 3 of the Hard Wire Quench Detector
7. Demonstrate that the Solenoid remains a viable superconducting magnet demonstrating original splice resistances and no turn-to-turn shorts.
8. Demonstrate soft ramp profile ramp-down to 0A while not tripping the Quench Detector over both current ranges.
9. Investigate if the Magnet Power Supply (MPS) in the "tuned to 25 H" is capable of being "Slow Dumped" while in a ramp to 140 A without tripping the Quench Detectors (QD)

Administrative Requirements and General Comments

- Perform all Solenoid Operations per the Operational Safety Procedure (OSP)
- Perform the remaining items in D000000402P007RevA Solenoid Pre-Power Up Checklist associated with cryogenics and vacuum.
- Calibrate the PLC Coil quench Detector and the Tap-Coil Quench detector per part 3 of D000000402-P005RevB.
- It is assumed that Revision B of this Commissioning Procedure was partially performed and that interlock verifications made under that Revision are still viable (If the circuitry was modified in the interim, revisit those interlock tests)

The Solenoid Distribution Box Helium Vessel shall be 60 % full of Liquid Helium per the latter part of Revision B of this Procedure in order to start Revision C.

- If the SOE System is repaired and operational for this test, verify that the SOE indicates the appropriate “first-fault” at every interlock test below. If SOE indicates incorrectly, note the circumstances in the Elog for the item and continue to the next item.
- The inoperative liquid helium level gauge’s hard-wire interlock is removed from the fast dump circuit and the PLC Fast Interlock Chain. A PLC slow dump from the differential pressure gauge system substitutes the level gauge interlock. Redundancy is not necessary for this test because the system is “manned” and monitored throughout the test period and other systems (vapor cooled lead voltage, vapor cooled lead lower temperature) provide similar redundancy.
- For this test, the cable break circuit in the Hard Wire Quench Detector shall be made inoperative. This removal of a marginal interlock is justified because the voltage it imposes across the coil circuit adds an unwanted, extra level of signal voltage complexity. Since the QD’s error signal is monitored continuously during this manned test, operators will be able to recognize if this obscure and unlikely cable break happens.
- For this test, the problematic Local Control Board on the MPS may not be installed. It exhibited intermittent failures during earlier tests. The best time to verify its good operation is during tests while the refrigerator is in repair. The Local Panel has two values: (1) It has a direct read-out of MPS and its interlock status that, when not available, can be queried from the Control Screen, a minor inconvenience. (2) The ability to aid in directly testing the PLC’s Current Limit is lost. The local mode is used to over ride current control. The solenoid still has two other current limits, enough for a manned test.
- Because of potential repeat of erratic readings such as obvious drift or spikes in readings while no current is in the magnet seen in the past, Coil 1 Strain Gauge SG2 (Right radial), SG 5 (Left radial) and Coil 3, SG1 (1:30 Axial) Heim column strain gauges may be commented-out during operations of the PLC Software Interlock that trips on excessive strain.

Final Vacuum System Checks

1. For all non-pumped coil-insulating volumes, is the key switch in “Closed” position and the key removed to the Key Safe?
2. For all pumped coil insulating volumes, (1) is the Turbo Pump up to 1000 Hz speed, (2) is the key switch in “Automatic” position and the key removed to the Key Safe?
3. Are pump-out valves on the Roots Valves at the Chimney, on the chimney vacuum gages and on the Side Port vacuum gauges administratively locked out?

Hardware Fast Dump Interlock Verifications

- The following hardware fast dump tests verify that hard-wired interlock systems, not tested under Revision B, operate as expected.



THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
JUNE 10, 2013

IMPORTANT!

Continuously monitor voltage taps during fast dumps for excessive voltages. Large voltage spikes (> 5 V) that occur during a fast dump may be an indication of an open dump circuit. If voltage spikes occur, halt testing immediately, determine cause of voltage spikes and mitigate as appropriate.

TURNING ON THE MPS

1. With the MPS locked out, opening the enclosure at the VCL, perform a sensitive resistance reading of the total solenoid coil across the top of the VCL. Elog the reading. The reading should be very near 123 $\mu\Omega$. If not, explain the discrepancy before continuing with the test.
2. Remove all "Buggers" in the system and log their removal in the ABIL System for Hall D under "Useful Links " on the JLAB Logbook page. Items that are "Commented Out" in the PLC software that are not explained in this Procedure are considered Buggers. The Division Safety Officer must approve any remaining Buggers.
3. Verify the jumper on the MPS Regulation Board (Jumper 1) is in its right-most or inductive position.
4. Voltage tap circuits, quench protection circuits, pick-up coils, PXi system and archiving system shall be operational. Turn on the PLC archive and PXi System, initiating a recording session named by the date and time.
5. Zero the PXi data logging system.
6. Set MPS front panel ("CEBAF") overcurrent set point to 25 A. Set Newport overcurrent detector set point to 20 A. Set PLC overcurrent limit to 20 A. Set slew (ramp) rate to 0.2 A/s.
7. Turn on the MPS. Reset so the Dump Contactor closes. The requested current shall be zero. Verify supply is turned on.
8. Observe if the transients still trip the QD upon Power Supply's turn-on.
9. If the hard wire QD trips, dis-engage the QD using the momentary switch and turn on the MPS again.
10. Re-engage the QD immediately after turn-on by letting go of the switch.
11. If the PLC QDs trip, disengage them using the green disengagement software button on the MPS Control screen, turning it to RED.
12. Immediately after the MPS has turned on, engage the PLC QDs, turning the button to green.
13. Use the methods of 7 through 12, to turn on the Power Supply, if necessary, for all future actions of this procedure.



THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
JUNE 10, 2013

VCL OVERVOLTAGE – Fast Dump

14. Reset the MPS. Simulate Upstream (US) VCL overvoltage using Voltage Tap Test Box. Verify initiation of fast dump by the US VCL Newport Controller. Verify SOE “VCL Overvoltage” if it is operational.
15. Reset the MPS. Simulate Downstream (DS) VCL overvoltage using Voltage Tap Test Box. Verify initiation of fast dump by the DS VCL Newport Controller. Verify SOE “VCL Overvoltage” if it is operational.

VCL FLOW CONTROLLERS – Fast Dump

16. Disable PLC VCL Flow interlock by setting VCL Interlock threshold to 0.0 SLPM.
17. Reset the MPS. Halt flow in upstream VCL mass flow controller by closing the associated valve. Verify initiation of fast dump by hearing Dump Contactor open. Verify SOE “VCL Flow” (if operational). Restore lead flow and turn power supply back on.
18. Reset the MPS. Halt flow to downstream VCL mass flow controller. Verify initiation of fast dump. Verify SOE “VCL Flow” (if operational). Restore lead flow and re-enable PLC VCL interlock by setting VCL Interlock threshold to 2 SLPM.

QUENCH DETECTORS – Fast Dump

19. Set the balance setting on all QD and PLC QDs to match the ratio of the inductances at zero current in elog [3154577](#). Disable the PLC Coil Quench Detector and the PLC Tap-Coil Quench Detector by setting their voltage thresholds to 10 V.
20. Reset the MPS. With all quench detector switches on the Test Box open (Toggle Down), simulate a quench using Voltage Tap Test Box on Channel 3’s Coil Sets and verify tripping around the 100 mV threshold. (plus and minus) (Note that QD Channels 1 and 2 are not be used during these tests.) Verify initiation of fast dump. Verify SOE “Quench Detector” (if operational). Set all the voltage test box toggle switches to up “closed” position and secure with tape.
21. Reset the MPS. Verify that the PLC Quench Detectors were qualified per D000000402-P005 Rev. B Solenoid Quench Detector Tuning Procedure Part 3. Re-enable the PLC Coil Quench Detector and the PLC Tap-Coil Quench Detector by setting their voltage thresholds to 100 mV.

LOWER VCL OVER TEMPERATURE – Fast Dump

22. Reset the MPS. Simulate VCL cold end over temperature by adjusting the relay set point for LakeShore #2, Channel #1 to 3 K. Verify initiation of fast dump. Verify SOE “VCL Over temperature” (if operational). Reset relay set point to 8 K.
23. Repeat Step 22 for LakeShore #2, Channel #'s 2, 3 and 4.



THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
JUNE 10, 2013

VACUUM CONTROLLER – Fast Dump

24. Reset the MPS. Test Coil 1 vacuum interlock by adjusting the relay set point for Coil 1's Cold Cathode vacuum controller to a value BETTER than the current vacuum pressure in Coil 1. Verify initiation of fast dump. Verify SOE "Vacuum Failure"(if operational). Reset relay set point to 1×10^{-5} Torr.

Repeat Step 24 for the remaining 3 coil and distribution box vacuum controllers.

HDR REFRIGERATOR INTERLOCK – Fast Dump

25. Reset the MPS. At the Refrigerator Control Screen, press the Test Button to test the Refrigerator PLC functionality for this interlock . Verify initiation of fast dump. Verify SOE "HDR Refrigerator"(if operational).

PLC Fast Dump Interlock Verification

The following steps test the PLC Fast dump items. For each test, verify that the SOE indicates the proper "first-fault" (PLC Fast Dump, in this case) (if operational).

PLC HIGHER HELIUM PRESSURE LIMIT – Fast Dump

1. Reset the MPS. Set PLC Helium Pressure Fast Dump limit to 0.9 Atm Absolute. Verify initiation of fast dump. Reset PLC Helium Pressure Fast Dump Interlock limit to 2.1 Atm Absolute. Note that successful trip also verifies that the PLC Fast Dump chain works.

PLC VACUUM LIMIT – Fast Dump

2. Reset the MPS. Set PLC vacuum limit to $<1 \times 10^{-10}$ Torr on each of the 5 Cold Cathode Gauge readings. Verify initiation of fast dump for each. Reset PLC Interlocks to $<1 \times 10^{-5}$ Torr.

PLC DIFFERENTIAL PRESSURE LIMIT – Fast Dump

3. Reset the MPS. Set PLC Helium Differential Pressure limit to 100%. Verify initiation of PLC Fast dump. Reset PLC helium Liquid Level Limit to 35%.

Hard Wire Slow Dump Interlock Verification

- The HMI MPS and Interlock screens should indicate which interlock tripped in tests below. Actual Slow Dump requires $>160\text{A}$ to trigger current going through the Thyristor. Below that current the Pass Bank still turns off, the dump switch remains closed but the Dump Resistor and diode absorb the energy. The only hardware indication that the Power Supply is in Slow Dump Mode is that the current starts declining at the fast dump rate but the dump contactor does not open (Only the



THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
JUNE 10, 2013

sound of the inlet power contactors is heard and there is no indication on the power supply display). Actual Slow dump functionality will be tested during higher current ramps.

- For each test below, verify that the SOE (If the SOE is operational) indicates the proper “first-fault”. If the SOE indication is wrong, note it in the elog and go on to the next item. Successful indication of Slow Dump is verified by decreasing magnet current and NO audible report from the Fast Dump Contactor.

VOLTAGE TAP CABLE INTERLOCK – Slow Dump

1. Reset the MPS. Verify that solenoid has zero current, but MPS is on. Disconnect Coil 1 Voltage Tap Cable from its current limiting resistor box. **DO NOT ATTEMPT TO RAMP WITH VT CABLE DISCONNECTED.** Verify SOE “VT Cable Interlock” and Interlock HMI Screen indicates Slow Dump (if operational). Reconnect Voltage Tap Cable.

INSTRUMENTATION CABLE INTERLOCK– Slow Dump

2. Reset the MPS. Verify that solenoid has zero current but MPS is on. Disconnect a Cable from the Instrumentation Cable String. Verify Cable Interlock Trip on Interlock HMI Screen indicate Slow Dump. Verify SOE “Cable Interlock” (If operational). Reconnect Cable.

CEBAF OVERCURRENT (MPS Panel) – Slow Dump

3. Reset the CEBAF (MPS Panel) Current Setting on the Power Supply to 10A. Reset the MPS. Soft Ramp to 15A. Verify initiation of slow dump as current passes 10 A. Verify SOE “CEBAF Overcurrent” Reset MPS front panel overcurrent limit to 25 A.

NEWPORT OVERCURRENT – Slow Dump

4. Reset the MPS. Reset the Newport Overcurrent detector current Setting to 10 A. Soft Ramp to 15 A. Verify trip of MPS as current passes 10 A. Reset Newport overcurrent detector set point to 20 A. (Newport overcurrent is not in the SOE.)

GROUND FAULT DETECTOR (GFD) – Slow Dump

5. Reset the MPS. Elog the setting limit for the GFD. Verify that the GFD is working by turning its adjustment limit to 0.00 V. Verify SOE “Ground Fault” is indicated (if operational). Reset limit to logged limit.

PLC WATCHDOG – Slow Dump



THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
JUNE 10, 2013

6. Reset the MPS. Disengage the connector from the PLC to the Watchdog Relay. Verify that Slow Dump is initiated. Verify SOE "PLC Watchdog" (if operational). Re-engage the connector.

PLC Slow Dump Interlock Verification

- The HMI MPS and Interlock screens should indicate which interlock tripped in tests below. Screen should indicate PLC Slow Dump.
- Use a Flagged "Test Jumper" to defeat the hard wire interlock corresponding to any respective software interlock.

PLC OVER CURRENT – Slow Dump

1. (Perform this check only if Local Mode is available.) Set PLC overcurrent set point to 10 A. Reset the MPS. Switch Power Supply to Local Mode. Attempt to ramp to 15 A using the Knob Control. Verify initiation of slow dump as current passes 10 A. Reset overcurrent set point to 20 A and switch MPS to Remote Control.

PLC VCL LOW FLOW – Slow Dump

2. Insert hard wire jumper in Upstream VCL interlock. Reset the MPS. Halt Upstream VCL flow. Verify initiation of slow dump. Reestablish flow through Upstream VCL. Remove jumper.
3. Insert hard wire jumper in Downstream VCL interlock. Reset the MPS. Halt Downstream VCL flow. Verify initiation of slow dump. Reestablish flow through Downstream VCL. Remove jumper.

PLC HELIUM HIGH PRESSURE INTERLOCK – Slow Dump

4. Reset the MPS. Set PLC Helium Pressure Slow Dump High interlock limit to 0.9 atm. Verify initiation of slow dump. Reset PLC Helium Pressure Slow Dump High Interlock to 1.4 atm –

PLC HEIM COLUMN STRAINS – Slow Dump

5. Reset the MPS. Set PLC Axial Column Force limit to 0.1 lbf. Verify initiation of slow dump. Reset PLC Axial Column Force limit to 20,000 lbf.
6. Reset the MPS. Set PLC Radial Column Force limit to 0.1 lbf. Verify initiation of slow dump. Reset PLC Axial Column Force limit to 7,500 lbf.

PLC FAST DAQ KEEP ALIVE – Slow Dump

7. Reset the MPS. Disconnect Ethernet cable from PXi. Verify initiation of slow dump. Reconnect PXi Ethernet cable.

PLC FAST DAQ TURN-TO-TURN SHORT – Slow Dump

8. Reset the MPS. Fake a turn-to-turn short from the PXi using the button on the PXi screen. Verify initiation of slow dump.

AC POWER LOSS – Slow Dump

9. Reset the MPS. Using web controls for UPS, open the contact for Relay 1 (indicating a loss of electrical power). Verify initiation of slow dump. Close the contact for Relay 1.
10. Remove any flagged Jumper.

Qualifying the Magnet and Commissioning Quench Detectors at 15 A

15 A QD TUNING AND T2T SHORT MEASUREMENT

1. With the MPS on, check that the offset of the Quench Detector is zero.
2. Disengage the PLC Quench Detectors using their expert panel button.
3. Disengage the Hard Wire Quench Detector with the momentary switch.
4. If the MPS was “tuned to 25H”, start a non-soft ramp to 15 A at about 0.012 A/s to observe if transients are still generated.
5. After any transients have died down, observe the error signal from the QD on a Fluke Meter, turning the Balance Pot for Channel 3 to reduce the absolute value of the error signal to near zero Volts (<0.1 V (absolute) on the error signal) if possible.
6. Engage the Hard Wire QD (release the momentary switch) if balance is (<0.1 V on the error signal) during steady ramping and engage the PLC QDs if voltages are below the thresholds during steady ramping.
7. Study the trip voltages of the PLC QDs for guidance in settings and sensitivities necessary to keep engagement during future ramps.
8. If transients that trip the Hard Wire QD are still generated as the ramp up is finishing, disengage the Quench Detector (If it was engaged) with the momentary switch when near to 15 A so as not to trip the QD. Disengagement may be necessary for the PLC QDs as well.
9. While at 15 A, observe the sum of the voltages across the coil from the bottom of the vapor cooled leads (VTT 3 through VTT 21). Calculate the resistance of the coil (actually its 113 splices) and Tap Coils. (Resistance across the Solenoid at the top of the VCL before the first test was 123 $\mu\Omega$.) Observe if there are outliers across any VTT and stop the test until they are explained.
10. Start a ramp to zero at a similar ramp rate using the similar procedures.
11. Only one non-soft ramp may be necessary to characterize if turn-to-turn shorts are not present as below.
12. Analyze the PXi Data to verify the Inductances remain the same as during initial commissioning.
13. Analyze the PXi Data for lag in magnetic field vs. current to establish that turn-to-turn shorts are not indicated.

14. If the “Tuned for 25 H MPS” (If available) is sufficiently without transients with a non-soft ramp, these ramps may be repeated with various ramps and settings of the balance pot to study the behavior of the Hard Wire QD and for different settings and sensitivities of the PLC QD. If transients are still produced, continue to the soft ramp below.

SOFT RAMP (AND TUNED POWER SUPPLY – if available) TESTS

Note that “soft ramp” means the soft start to a ramp process where the start and end of a ramp is accomplished in several stages where each successive stage consists of a higher slew rate for a time period. The inverse slew structure holds for slowing the ramp to constant current. Ramping down is a mirror image of ramping up.

15. Initiate soft ramp to 15 A at stages to be worked out during these tests. The object is to assess if voltage tap transients are reduced such that the QD error signal doesn't exceed 5 V.
16. Leveling off the current may need additional programming or manual intervention by the operator to achieve the goal of not tripping the quench detector as the power supply stabilizes at a set current.
17. Observe if the QD's 5 V trip limit is exceeded (at the sensitivity settings ~150 mV now set), leading to a fast dump upon start of ramp. If so, try other combinations of stages and final slew rates to not exceed the trip limit. Also try raising the value of the sensitivity setting to at least get a ramp started, backing off to original settings as experimentation with the stages allows. Operator may also try biasing the error signal to the opposite side of the limit using the balance adjustment and try a ramp again. (The latter solution may not work for the soft ramp to lower current.)
18. PLC's Coil and Tap-Coil Quench Detectors shall be qualified for use during the above hard wire tests. They may be turned off during the hard wire qualification and then turned on in order to be commissioned.
19. Observe if the inductive Tap-coil Voltages recorded in the PXi are consistent with former readings.
20. Observe that the GFD didn't trip.
21. Ramp down to zero current using the soft ramp that was developed, by the operator (or programmed).
22. Soft Ramping may, or may not, be successful in not exceeding the QD error signal limit of 5 V or in not tripping the PLC Quench Detectors.
23. If the QD commissioning is not successful and further testing is delayed, turn off the PXi Data logging.
24. If commissioning of the Quench Detectors is successful, continue the test.

Qualifying the Magnet at 140 A

1. Voltage tap circuits, quench protection circuits, pick-up coils, PXi system archiving system shall be operational. Sequence of Events Monitor (SOE) may be operational
2. Set two Current Limits (1) Newport Controller, (2) PLC Software limit to 145 A. Set the (CEBAF) Power supply Limit to 150 A (higher because of low resolution of read-out)
3. Zero-Out Strain gauge readings

4. If the PXi was turned off, turn on the PXi System, initiating a recording session named by the date and time.
5. Zero the PXi system.
6. Turn on the MPS and reset at a requested current of zero. Using the soft ramp.
7. Ramp to 30 A using the soft start ramp.
8. This ramp validates the ability of the hard wire and PLC QD to operate under the soft ramp conditions to higher currents than 15 A.
9. Verify that the PXi inductive voltages recorded match the inductances anticipated.
10. If the ramp causes QD trips, or voltages are not as anticipated, debug the systems until success.
11. Soft Ramp to zero A.
12. If the MPS has been tuned to 25 H, Soft Ramp to 30 A. At the 15 A current point, initiate a slow dump. Determine if voltage spikes are initiated such that the QDs initiate a fast dump. Allow the current to return to zero A. Skip this step if the MPS is not tuned.
13. Reset the MPS. Ramp to 140 A using the soft ramp.
14. If the ramp causes QD trips, debug the system until success.
15. Observe the following for odd behavior:
 - a. Hard wire Quench Detector error signal,
 - b. PLC Quench detector signal noise behavior,
 - c. Support column strain gauge readings,
 - d. VCL voltage and temperature readings,
 - e. Voltage tap readings during ramp and at flat top,
 - f. Monitor LHe level and valve position history looking for increased usage,
 - g. If necessary, follow-up with de-bugging and additional ramps.
16. The final ramp shall remain at current for 20 minutes.
17. While at 140 A, observe the sum of the voltages across the coil from the bottom of the vapor cooled leads (VTT 3 through VTT 21). Calculate the resistance of the coil (actually its 113 splices) and Tap Coils. (Resistance across the Solenoid at the top of the VCL before the first test was 123 $\mu\Omega$.) Observe if there are outliers across any VTT and stop the test until they are explained.
18. Ramp down to zero current using the soft ramp.
19. Observe the following for odd behavior:
 - a. Hard wire Quench Detector error signal,
 - b. PLC Quench detector signal noise behavior,
 - c. Support column strain gauge readings,
 - d. VCL voltage and temperature readings,
 - e. Voltage tap readings during ramp and at flat top,
 - f. Monitor LHe level and valve position history looking for increased usage,



THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
JUNE 10, 2013

- g. If necessary, follow-up with de-bugging and additional ramps.
- 20. Turn off the MPS.
- 21. Stop the PXi archive and reduce the archive rate of the PLC data.