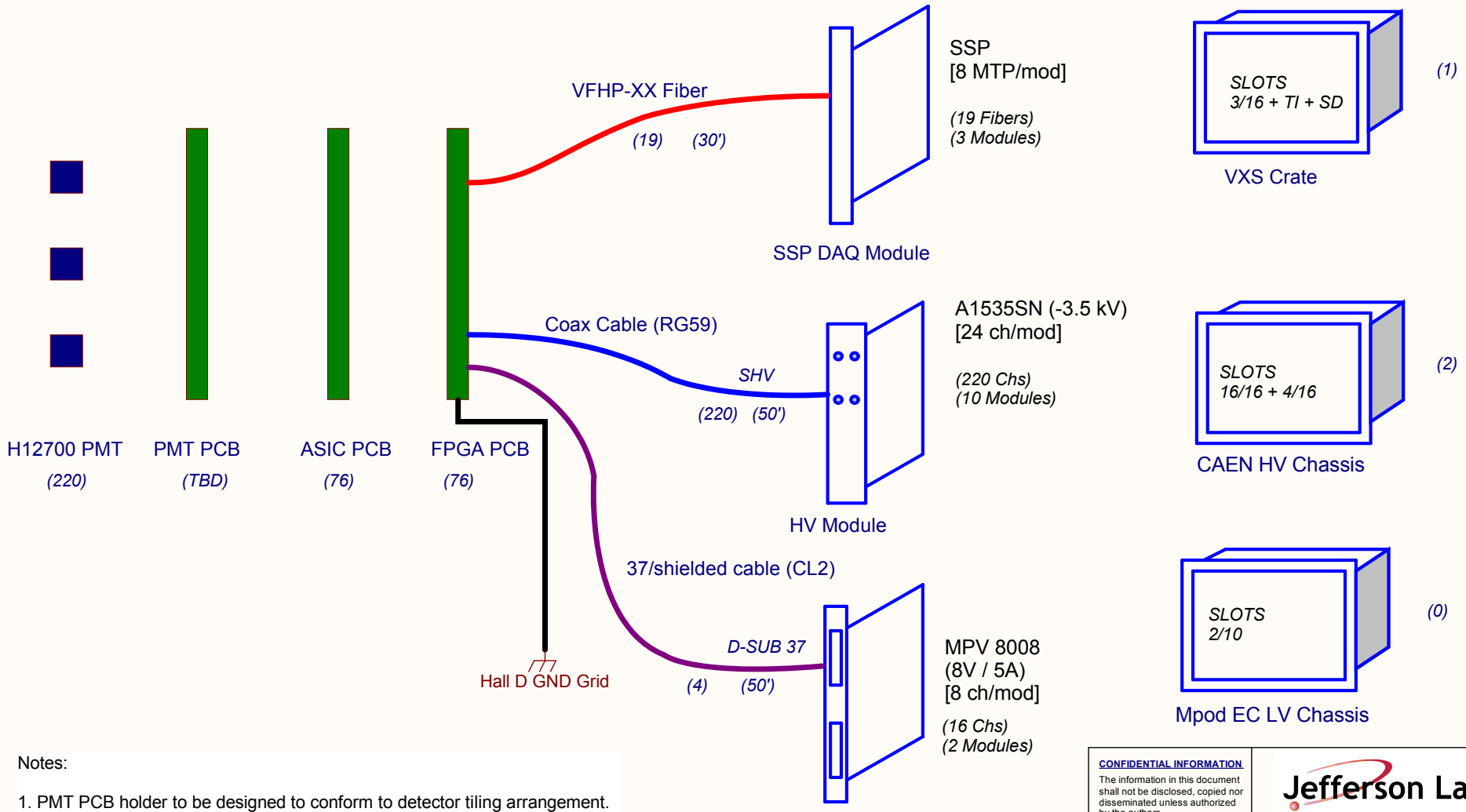

Notes:

1. PMT PCB holder to be designed to conform to detector tiling arrangement.
2. One VFHP-XX fiber serves 4 FPGA PCBs.
3. One HV channel per MAPMT.
4. MPOD LV chassis slots available and located at D2-5-MID.
5. All supplies are floating, referenced to GND grid at detector.
6. GND connection(s) with insulated 4/0 primary or 2 AWG secondaries.

Jefferson Lab

Drawn: *	Date: 6/18/2015	Title: Hall D DIRC Readout Block Diagram	
Checked: *	Date: *		
Approved: Preliminary		Size: B	Drawing Number:	Revision: *
Engineer: FJ Barbosa		File: C:\Users\barbosa\ALTIUM\DIRC\DIRC Block Diagram\DIRC Block Diagram.SchDoc	Sheet 1 of 1