12GeV Trigger meeting notes:

22 Jan 2010: C. Cuevas, H. Dong, J. Gu, J. Wilson, E. Jastrzemski, B. Raydo, A. Somov

15 Jan 2010: C. Cuevas, H. Dong, J. Gu, A. Somov, J. Wilson

8 Jan 2010: C. Cuevas, H. Dong, J. Gu, A. Somov, J. Wilson

18 Dec 2009: C. Cuevas, B. Raydo, H. Dong, J. Gu, E. Jastrzembski,

Updated prototype board status table:--22 January 2010

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** **SN001 ----------** **SN002 ----------** **SN003 ----------** **SN004 ----------** **SN005 ----------** **SN006 ----------** **SN007 ----------** **SN008 ----------**	 **Daq Lab F110** **Daq LabF110** **Daq Lab F110** **EEL – 126** **EEL109** **Hall C** **Hall A** **EEL – 126**	 **Test Board** **OK Hall A Student** **Moller Spare** **FDC test setup** **Needs repair** **Dave Mack & Steve Wood** **Moller setup** **FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded** **Sent to IU for FCAL testing** **12Oct2009**
4	**Trigger Interface** **Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** Front Panel – Signal Distribution	**EEL109/DAQ Lab**	**Complete** **Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Testing complete**

0. Trigger/Clock/Sync – TI/TD

22 January 2010

FastTrack schedule has been created to show the activities associated with the design of the latest Trigger_Interface-Trigger_Distribution module. There are two other peripheral modules that are listed in the activity schedule and they are part of the TI development and also include fanout of the TI signals to the CAEN V1290 TDC.

8 January 2010

Progress on the new TI/TD module was reported by William. The schematic work and initial component placement have started, and there will be details to resolve for the mechanical placement of a mezzanine board that will be used if a TI/TD board needs to be used in a legacy system.

William updated the status of the distribution module that will be needed for the Hall B CAEN 1290 TDC units. These TDC do not use VXS, so a distribution module has been specified and the design is progressing nicely. Up to 16 V1290 units will be connected to the distribution

module. This distribution module will receive the clock, trigger, and synch signal from the TI via P2.

William, Ed and Chris met 'offline' to discuss the activity and preliminary schedule for the TI/TD project and Chris will generate a FastTrack schedule and add this project to the overall Trigger System schedule.

December 2009

We discussed the design concept for the production version of the trigger interface and trigger distribution module. William presented details of this design concept at the Hall D Online meeting and there was an enlightening discussion. Highlights of the discussion below:

- ➔ One circuit board design for TI and TD functions.
- ➔ Fiber transceivers will be populated depending on the TI board features that are required.
- ➔ Local subsystem crates can be connected together and one TI would operate as local TS
- ➔ Front panel I/O will occupy transceiver area, so initial assembly will determine what types of board features are available.
- ➔ Cost issues must be considered for TD and multiple transceiver versions of the TI. There are a limited number of subsystem configurations so the most cost effective TI version will only need 1 transceiver. Most of the sub-system crates will be in close proximity to each other, so expensive 12 fiber ribbon cable and transceivers may not be necessary.

At the Hall B collaboration meeting a new board requirement was declared for the Caen TDC. There will have to be a module that occupies a payload slot and distributes the required signals to the front panel of up to 16 Caen TDC. A simple specification sheet is needed and this module receives signals from the SD and P2.

- ➢ Decision for P2 I/O for the FADC250_V2 and F1TDC_V2 has been declared. There is NO need for P2 I/O connections because we have front panel distribution modules for Users that want a small number of modules for a lab test setup. If the Users need more modules in a test setup then they will use a full sized VXS crate and use the standard method to distribute the common signals to each payload board.

1. FIRMWARE TESTING

22January 2010

Ed has been working on firmware development and transferring his VME SST readout code from Altera HDL (AHDL) to Standard VHDL that will be used on future designs. This code change will allow the firmware to be used on virtually any FPGA and not solely for Altera devices. Progress is going well and at some point soon, the latest VHDL version will be tested and verified.

8 January 2010

No new firmware issues have been reported and Ed has been busy with converting the VME SST firmware from Altera 'HDL" to standard VHDL. This new VHDL version will need to be verified and will be used on virtually all new VXS payload modules.

There will be a number of firmware activities started once the SSP prototype module is assembled later this year, and William will also join in the development of firmware for the TI/TD units.

December 2009

All firmware issues have been resolved and tested by Ed and Hai. These firmware revisions have been uploaded to the specific FADC250 boards that are in use by several groups. See prototype board status table for board location details.

IU FCAL group is working with the timing algorithm. A few questions have been exchanged and they hopefully should have results soon.

2. *SUB-SYSTEM PROCESSOR (SSP)*

22January 2010

Progress is ahead of the planned schedule and we talked about ordering components that show list a long delivery. We may be able to combine orders now for the fiber transceivers needed for the SSP and possibly the TI/TD prototypes. It is still too soon to create a final bill of materials.

The next stage of the board design is configuring and optimizing the auto-router. There will be plenty of time for post layout verification before ordering the bare boards. The 16 channel discriminator module has taken a higher priority for now, but soon enough the SSP will become the highest priority.

January 2010

The schematics for the SSP have been closely reviewed by Ben and Chris and the board placement activity is complete. This board is ready for routing and any long lead components should be purchased as soon as possible. The test plan for the SSP should also be drafted soon, and there are several trigger applications that have been proposed by the CLAS12 folks that will need to be reviewed before developing new firmware. The Hall D requirements for the SSP have been declared and reviewed, and give a firm starting point to test the performance of the SSP functions.

December 2009

The design of the SSP is ahead of schedule and the placement of the components on the payload board has been completed. Setting up the best board routing strategy will be the next activity and Ben has already performed functional simulation of the initial firmware. The transceiver protocol between CTP and SSP has been developed also.

The bill of materials has been reviewed to see if there is a way to consolidate the FPGA or other common components that will be used on other board prototypes. The BOM should also be reviewed and long lead items should be ordered soon.

Review of the schematics and functional descriptions/specifications/requirements has been requested. Chris (and others) will need to review these documents and check for consistency with other modules planned for the global trigger crate.

3. CUSTOMERS

22 January 2010

We had a short discussion about the recent problems with several channels of the 12bit FADC250 module. Hai is convinced that the problem is associated with the tight setup & hold timing specifications for the Maxim 12bit part. There is little margin, and these timing issues may be creeping up because of temperature fluctuation. We do not believe we have seen these types of issues at Jlab with this unit, and the number of channels that are working are enough for the FCaL group to use for testing.

8 January 2010

→VME64x mini crate and new GE Fanuc CPU have been shipped to IU. The FCAL group has been using the VXS crate that was loaned to Gerard and Gerard needs the crate to finish testing the FDC flash modules. There has been recent work and a few troubleshooting questions from the IU folks when using the latest 12 bit FADC250, and hopefully these issues will be resolved without having to send the unit back to Jlab for testing. Looking forward to the results from the timing extraction algorithm!

→The Hall C folks have not stopped by to pick up the test crate and FADC250 module yet. I will ask them one more time and then see what other group could use the module. I have a request from the Accelerator Injector group so we will see.

→No recent news from the Moller folks in Hall A. I believe they are on track to use the module for Prex coming up in March.

December 2009

Report that the IU FCAL group had sent a few questions regarding the latest timing extraction firmware that was updated in the 8 channel, 12bit version of the FADC250. Sounds like they are actively setting up to test the new timing algorithm and will be able to verify the results soon.

Hai and Ed have updated all firmware versions for the Moller application and the other flash boards have all been updated and tested.

4 "B" Switch - Signal Distribution Module (SD)

8 January 2010

The SD module will need to be revised to reflect the changes to the signal pair mapping for the front end crates. We have two modules in the lab and I believe we can modify these units to work for testing the SSP prototype and revision 1 of the FADC250 that will be ready before the end of FY10. The SD module revisions are effectively only signal pair changes and there are a few other circuit changes that will also need to be included for the final production lot.

December 2009

No significant updates to report. Stay tuned as this module will need to be updated soon.

5. System Diagrams & Test Stand Activities

22 January 2010

The front end crate pair map and global trigger crate map have been updated to reflect the latest decisions for signal interface between the TI and the front end modules. Same note for the global trigger crate, where the TI will interface to the GTP. The Trigger Supervisor crate will also need a signal pair mapping diagram to show how the SD and TD modules will communicate.

8 January 2010

This would be an appropriate place to note the discussion and ideas to test and commission the overall trigger system with simulation data that is loaded directly to the front end FPGA on the flash modules. The method to load these test data to the FPGA through VME has been developed, and there will need to be some software that can assemble and read the simulation data so that the front end channels are loaded properly for a given trigger system test.

Test patterns for a given sub system, would be loaded to the flash boards, and the SSP and GTP would be programmed to trigger if the given test pattern meets the trigger equation criteria. There are numerous possibilities here, and it was proposed to start with the development of software that would read and assemble data from a 'Physics' simulation, and process this data to the front end FPGA through VME. This development effort could start soon, and will certainly be essential once the trigger system is installed in the hall(s). Comments welcome and more discussions will follow.

December 2009

The front end VXS crate pair mapping diagram has been updated and this latest revision should be considered the final assignment. Collaborating institutions are requesting the pair map which includes signal level descriptions and pair polarity. The crate pair mapping is different from the original prototype design, and we have made these changes to accommodate the different modules for both the front end and global trigger crates and modules. For example, the TI module pair map is critical and has been finalized so that it accommodates the

GTP modules that will reside in the global trigger crate. Other pairs from the SD to the payloads have been changed to accommodate new requirements for additional signals.

Crate Trigger Processor (CTP)

CTP activities are complete.

6. Projects for FY10

22 January 2010

The GTP specification exists and has not been updated for several months. The activities for the schematic and detailed design issues have not been started and this may slip because the plan was to have a new hire in place by now. Starting the schematic and other activities *could* start soon, but it will impact other project assignments and I do not want to have that happen at this point.

8 January 2010

→Project schedule updates have been reported to the project management team. It has been noted that funding for procurements in the BIA activities are missing, so allocating funding for the purchase of prototypes for SSP, TI/TD etc will have to be extracted from 12GeV funding or a combination with 6GeV operations accounts.

December 2009 Projects are still progressing well and on track. Review schedule in Jan 2010.

ACTION ITEMS: **Next meeting → Friday 5 FEBRUARY 2010 at 11:00am in F226**