Trigger Supervisor

Trigger Supervisor History

- First TS specification draft: 2008 (TS_rev2 extension)
- Schematics/PCB started Oct. 2010 (TID expansion of TS functions)
- First ‘working’ meeting Monday, May 16, 2011 (working: deal with real issues)
- Future: merge the two

Trigger Supervisor PCB implementation

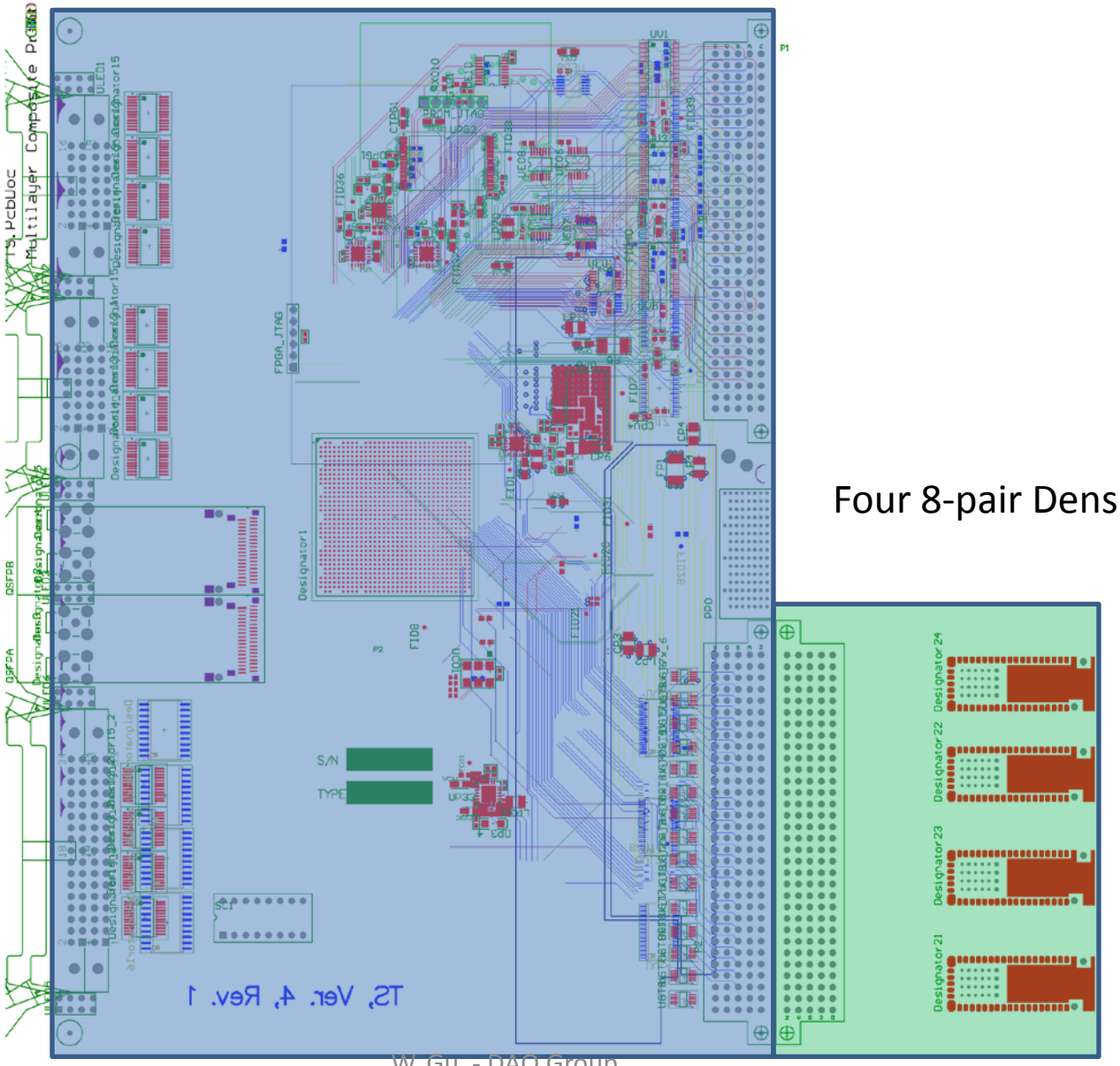
Front Panel

Four 2x8 (for trigger inputs)

Six quad-LED

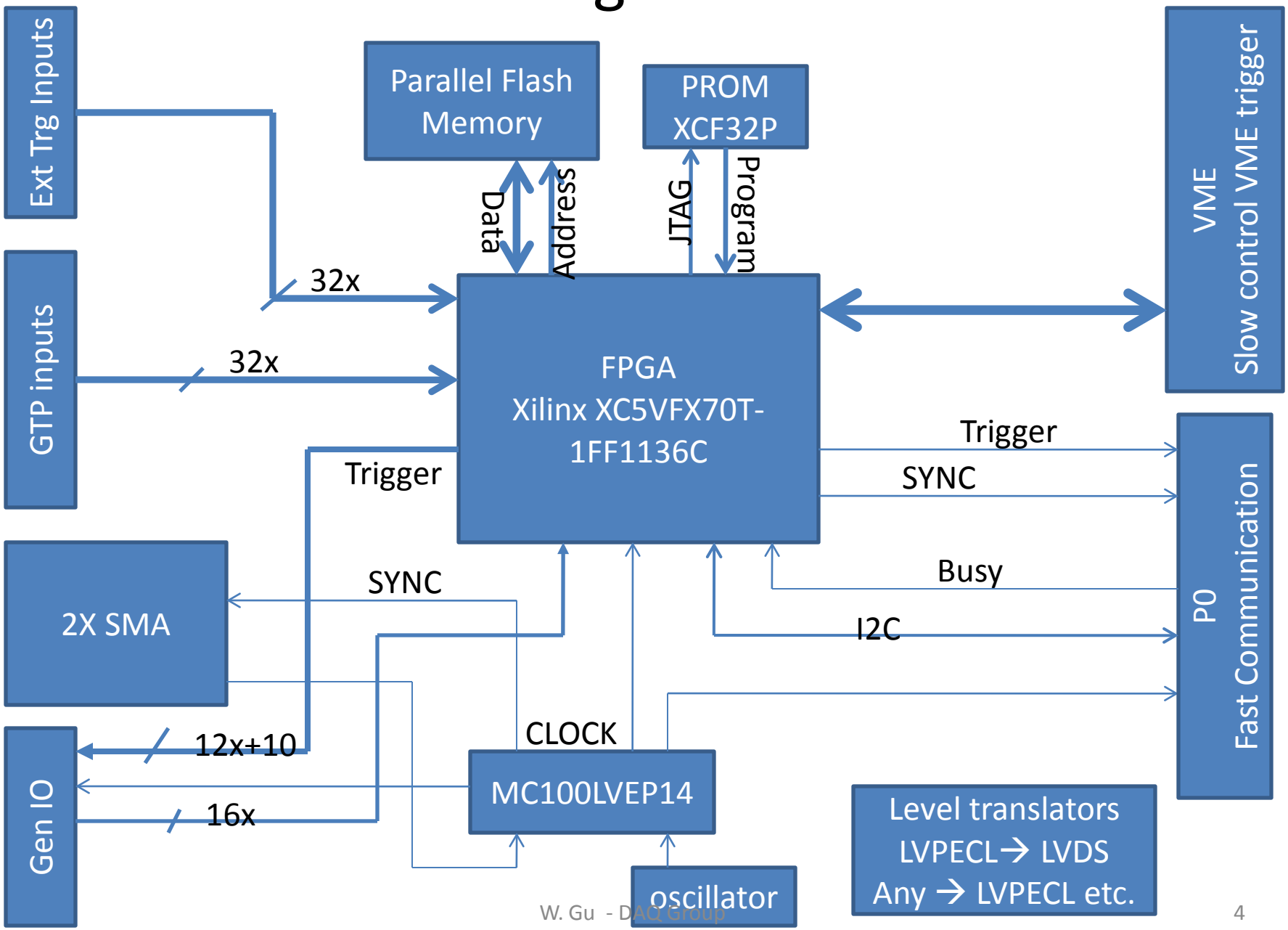
CLK I/O

Two 2x17 (for generic inputs and outputs)



Four 8-pair DensiShield

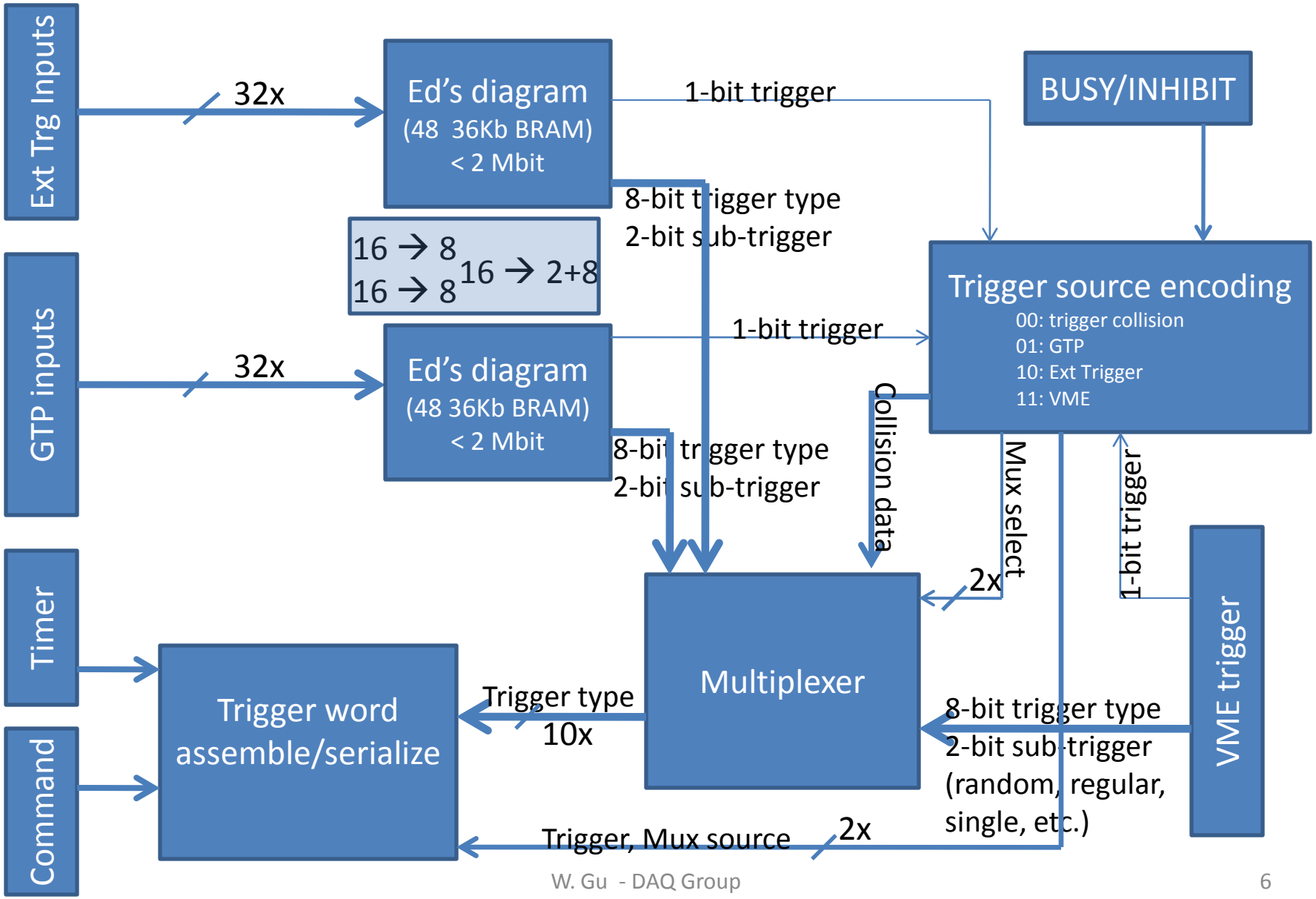
TS diagram


Ext Trg Inputs
Parallel Flash Memory
PROM XCF32P
VME Slow control VME trigger
Data
Address
JTAG
Program
GTP inputs
32x
32x
FPGA Xilinx XC5VFX70T-1FF1136C
Trigger
Trigger
SYNC
Busy
I2C
P0 Fast Communication
2X SMA
SYNC
CLOCK
12x+10
16x
Gen IO
MC100LVEP14
oscillator
Level translators
LVPECL→ LVDS
Any → LVPECL etc.

Component selection

3M Condo connectors: one 2x34, two 2x16
    32 external trigger inputs, 16 generic differential inputs, 12 generic differential outputs, 8 generic single-ended outputs
SMA RF connector: four: differential CLOCK input/output;
FPGA: Xilinx virtex-5, FX70T-1FF1136C: deep discount when buy with flash ADC
    5 Mbit block memory, 16 GTX, 640 I/O, 1 CPU
GTP input buffer: Micrel SY55855, dual LVPECL→LVDS buffer
Front panel input buffer: Maxim MAX9602, quad 'any-level'→LVPECL (V_{cco}=2.5V)
Front panel output buffer: On-Semi MC100EP91, triple 'any positive' → ECL;
    Plus, eight LVCMOS25 directly from FPGA;
P0: CLOCK/TRIGGER/SYNC to SD (LVPECL)
P1/P2: VME64x
P2: GTP inputs, compensate for the GTP routing delays (!)
Distributed LEDs on front panel: six quad-LED.

Trigger word generation



Sync word generation

The SYNC word generation will be the same as current TID implementation.
(moving the function from current TID to TS)

Clock generation

Oscillator (or external clock input, beam?) as the main source,
FPGA generates slower clock, which can be synced with TIDs (using AD9510)
using SYNC signals