12GeV Trigger meeting notes:

24-Aug-2012: C. Cuevas, B. Moffit, B. Raydo, W. Gu, J. Wilson, S. Kaneta, A. Somov

17-Aug-2012: C. Cuevas, B. Moffit, B. Raydo, N. Nganga, W. Gu, J. Wilson, E. Jastrzembski

10-Aug-2012: C. Cuevas, B. Moffit, B. Raydo, N. Nganga, J. Wilson, H. Dong, W. Gu, S. Kaneta

3 Aug 2012: Cancelled

27-July-2012: C. Cuevas, B. Moffit, B. Raydo, N. Nganga, A. Somov

20-July-2012: C. Cuevas, B. Moffit, B. Raydo, N. Nganga, A. Somov, E. Jastrzembski, Beni Z.

13-July-2012: C. Cuevas, H. Dong. B. Moffit, S. Kaneta, B. Raydo, N. Nganga, A. Somov, E. Jastrzembski

6 July 2012: No meeting

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0. Trigger/Clock/Sync – TI/TD

24-Aug-2012
→1st article shipping this week. Should receive boards week of 27-Aug.
→Acceptance test procedure not released, but William is prepared to verify the functionality of the new assemblies.
→Probably a good idea to post the test procedure so a few other folks become test 'experts'
→2nd TS prototype board has been used to test the partitioning feature. Progress is being made.

17-Aug-2012
→No news from CEM which is not bad news.
→TID or TI? What identifies the board difference?
--Front panel label:
--Firmware version is read from register
→Initial 15 units can be configured as TI or TD. The boards will require component rework at JLAB for proper TI or TD configuration.
→Production units will be assembled as TI or TD and identified with labels on the PCB.

10-Aug-2012
→CEM has made phone contact! Some change request for silkscreen.
→Delivery of 1st article boards remains the same; 22-Aug.
→Setup 1st article test stand in the DAQ lab.

27-July-2012
→Still on schedule for 1st articles.
→We have two prototype TS boards.
→We need to order components to assemble the second GTP prototype board.
→Order a full set of Densi-Shield cables
→Send second GTP prototype board for full assembly
→D. Abbott, B. Moffit, and William will begin development/discussions on implement the partitioning/control functions for the TS.

20-July-2012
→TI boards returned from the PEPPo group
→TI-TD Production order status:

-NO feedback from CEM yet, but scheduled delivery for 1st articles is 22-Aug. (15 TID units)
→Discussion about ordering TS "pre-production" boards before the end of August.
-Specification needed
-Consign parts or not?
-Finish and check schematic changes and board layout before ordering.

13-July-2012
→No status update for 1st article boards

1. *SUB-SYSTEM PROCESSOR (SSP)*

24-Aug-2012
→Zentech wins the award. 1st article delivery will be due after the vendor receives the fabrication files. BOM will be ordered, and schematics/Gerber will be ready for review soon.
→18 layer board! A new JLAB record.
→Board will use new fiber transceivers (QSFP)

17-Aug-2012
→Not officially awarded, but bidders have been evaluated and lowest cost selected.
→Schematics complete and will be reviewed.
→Layout is progressing well and will need careful check before sending to vendor for 1st article build.
→Firmware files have been sent to the Saclay folks and more discussions/meetings will develop for final implementation plans.

10-Aug-2012
→Production SSP boards will use new Avago Transceiver (40 GB) QSFP
→Savings of $35K!!!
→SSP has been awarded but not publicly released
→Schematic changes and board layout is progressing well
→1st article delivery will be based on when the fabrication files are ready
→Coming soon, new front panel

27-July-2012
→RFQ has been created for the SSP production order
→Transceiver award has been ordered
→Schematics and firmware has been sent to the Saclay group. The Saclay group is planning to use the SSP to readout the uMegas detector. (SSP in 32 'fiber channel' mode)

20-July2012
→Production order has been approved!
→2 week period for quotations
→Fiber transceiver order has been approved. These units are for ALL SSP and CTP modules.
→ECOs are 70% complete. Final checks in a few weeks and will coincide with reception of quotations.

13-July-2012
→PR has been signed and quotes are in the queue
→Total number of SSP will be 25 (All Halls)
→ECO activities are in progress.

2. CUSTOMERS

24-Aug-2012
→No boards to the Hall B PCAL group yet, but request has not reached an urgent state.
→A quick meeting with the Hall A folks produced a request for another FADC250, and other trigger hardware for their Compton detector test station. Orders for SSP and CTP were requested also and should be added to new contract orders.

17-Aug-2012
→Same note as 10-Aug.
→Crate and other modules sent to UConn for Tagger electronics testing.
→Use a TD (production version) in the Global Trigger crate test
→2nd FADC250 pre-production board given to Brad S. (Hall C) for detector testing in EEL-126

10-Aug-2012
→PCAL group to receive at least one FADC250 and a front panel distribution board
→No news is good news, and the Hall C folks are happy for now. (Or everyone is on vacation)

20 July 2012
→UConn will receive a full VXS crate for their testing activities. Hall D VXS crate inventory is almost complete, so a new crate can be loaned/shipped soon.
→Sergey will return from vacation soon, and the Hall B PCAL group will want to start cosmic ray studies with the PCAL and FADC250 boards. (EEL-125; shower curtain area)

13-July2012
→2nd FADC250 board returned from PEPPo and will be given to Brad S.
-Front panel fan-out and crate have been delivered to EEL-126
-Latest firmware can be downloaded if necessary

3. "B" Switch - Signal Distribution Module (SD)

24-Aug-2012
→No report. Nick will return 4-Sept.

17-Aug-2012
→Delivery of production boards will be mid-September
→No issues as far as we know
→Test procedure is in good shape, and minor edits have been added the documentation.

10-Aug-2012
→Balance of the order is due in September.
→Will need to keep the FADC250s, CTP and TI together for production testing
→CTP firmware modified and tested and works with the SD automated test procedure.

27-July-2012
→SD acceptance test procedure is complete, sin CTP. Testing is complete for 10 production units.
→In the spirit of continuous upgrades and feature upgrades, the SD firmware could be developed to handle the trigger_Out bits from the FADC250 boards in some majority logic or other functions. One other feature upgrade is the SD→TI data link.
→VME remote firmware download feature is a work in progress.

20-July-2012
→Acceptance letter has been sent to CEM, and the production order will proceed.
→Within 60 days we should start receiving the rest of the production lot.

→Test procedure is complete and there are a few enhancements to be tested.

13-July-2012
-->9 of 10 1st article boards have passed acceptance testing. A few resistors were identified as bad and cold solder joints identified, so there are a few minor assembly issues. 10th board requires the power connector.
→Discussion about including CTP register readbacks for the complete SD test.

4. System Diagrams/Fiber Optics

24-Aug-2012
→PO issued to Tiger Controls for the Hall C system. Prices were slightly lower than expected. Large order for Halls D & B should bring prices even lower.
→Fluke MTP fiber test equipment has been purchased. Due in 3-weeks.

17-Aug-2012
-->PR for Hall C is written and in the system, but not sent yet. Need to verify total cost etc, with Brad S.
→Halls D & B will share the cost of the Fluke MTP fiber optic test unit. (Scott's the owner)

10-Aug-2012
-->PR needs to be submitted to purchasing by end of August.
→Still have not received pricing from vendors.

20-July-2012
→Patch cables and panels will be ordered before 15-Aug Price estimates and details on part numbers for patch panel hardware and patch cables from two companies have been received.

13-July-2012
→Radiated fiber test completed. Should document the test and include details of fiber type, length, location, estimate of dose, etc.

5. Two Crate DAq test configuration

24-Aug-2012
→Time to get the hardware mounted in the rack:
--1st crate – Global – SSP (FADC250), GTP, SD, TI
--2nd TS, SD, TD
--Densi-shield cables. Use two cables for now (15 trigger bits + clock)

17-Aug-2012
→Scott continues to test the GTP using FADC250 boards as the data generators. VXS Gigabit serial links are running @5Gb/s with a few errors, but long term data is needed to increase our confidence level to operate at the higher bit rates.
→No VME backplane readout is exercised during the serial tests, and 2eSST readout should be exercised during the 5Gb/s serial data transmission testing to replicate a real system test. What should the duration of the testing?

10-Aug-2012
→16 FADC250s used as data generators to GTP @5Gb/s with some errors, but over a 48 hour period. Good news. No equalization parameter adjustments yet, but this could be tested and documented.

20-July-2012
→Scott presented a test scheme drawing a few weeks ago for the global trigger module/crate test. Preliminary register/command list needs to be described to Bryan. TS library is in place

(preliminary) and by next week (23-July) we should have this test setup to measure the last latency 'link'.
-Use FADC250 as data generators to GTP
-Use TD to distribute triggers
-Run realistic final trigger equation on GTP to simulate processing time.

13-July-2012
→Two crates will be available late next week so the global crate tests can be started.
→Use FADC250 boards as data generators to GTP and 2nd crate will have the TS, SD, and TD

20-JAN-2012 (Keep this date to reference full DAq crate procedure)

3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!

16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

Crate Trigger Processor (CTP)

24-Aug-2012
→Hai is on vacation and the bid packages are due 30-Aug
→Routing and placement are progressing well. Power fan-out and plane layers going well.
→Lowest price wins!

17-Aug-2012
→RFQ is on the public site and we have started to receive questions.
→Bid packages for the thirty-two (32) production boards are due 30-Aug-2012.
→New circuit board routing is progressing
→CTP production acceptance test stand procedure and firmware is under development
→CLAS12 CTP requirements. We want to develop CTP to use all 4 'lanes' from FADC250 boards. Imagine (6.25Gb/s *4 *0.8) data rate! Many things to discuss, but the CLAS12 folks have a great deal of experiments that will require higher bandwidth and trigger functions that will exceed the Hall D CTP design.

10-Aug-2012
→Project has started. Mountain of routing work.
→Ready for RFQ, paperwork signed and delivered
→Automatic test procedure will be developed.

27-July-2012
→Jeff has not started the routing yet, and will be busy with the F1TDC project for at least another week.
→PR has been approved for 32 units. (Hall D=30, Hall C=2)
→RFQ will be a few weeks

20-July-2012
→PR for 30 Hall D units has been sent for approval.
→Schematics complete
→Routing for new changes will start soon. (Jeff)

13-July-2012
→PR and specification finalized and need the signatures soon. (Chris' queue)
→Order will be for Hall D quantities only (+spares). Includes upgrades FPGA devices.
→CLAS12 CTP effort will need to be discussed further and regular meetings will begin as soon as Sergey returns from holiday.

GTP and Global Crate Developments

24-Aug-2012
→2.5 days running @5Gb/s with 16 FADC250 boards without errors recorded.
→The serial tests are performed without VME bus activity
→Serial testing should be performed with VME bus activity
→Embedded controller on the Altera part to manage serial testing? Sidetrack,
→GTP driver development started. i.e.(I^2C control, etc)
→Final Physics equation loading? Are we going to use Playback mode?

17-Aug-2012
→Full crate testing with 16-FADC250 boards @5Gb/s from all boards. BER data will be collected for the long test durations.
→Assemble 2nd prototype GTP. Quote from Advanced Assembly in the queue.
→Densi-Shield cables on order. Delivery date?
→Keep pushing forward to get the Global Trigger system configured and tested.

10-Aug-2012
→Full crate testing with FADC250s and GTP
→Radiated fiber has been tested. See results
→GTP second board assembly quotes are coming in and some parts may be consigned

27-July-2012
→VME download firmware will be used to configure the GTP (Global Trigger Crate) testing.
→Ethernet development is a lower priority but hardware functionality is correct
→Activities for ordering components and turn key for the 2nd GTP assembly will increase soon.
→Fluke fiber (MTP) test device will be loaned for a few days for evaluation.

20 July 2012
→After a few discussions, the 2nd prototype GTP board will be sent for assembly. Components will need to be ordered and the existing partially assembled items will need to be removed.

***ACTION ITEMS*: Next meeting - Friday 31 August @ 10AM in F226**