TAGH HV Scan Analysis

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Goals

1. Parametrize dependence of ADC-pulse-height on applied voltage in order to balance gains

2. Determine optimal operating voltages

   - Optimize in terms of timing resolution and tagger efficiency

HV settings history

- Fall 2014 run: started with all voltages set to 900 V
- Large channel-channel variations of fADC pulse-heights were observed, many overflows
- Dec. 2014: first attempt at gain balancing
  - Interpolated 800 V and 900 V data points
  - Pre-subtracted pulse-peaks set to 1550 counts
  - (Average,StdDev,Min,Max) HV: (820,37,747,950) V

Scan Dataset (Fall 15)

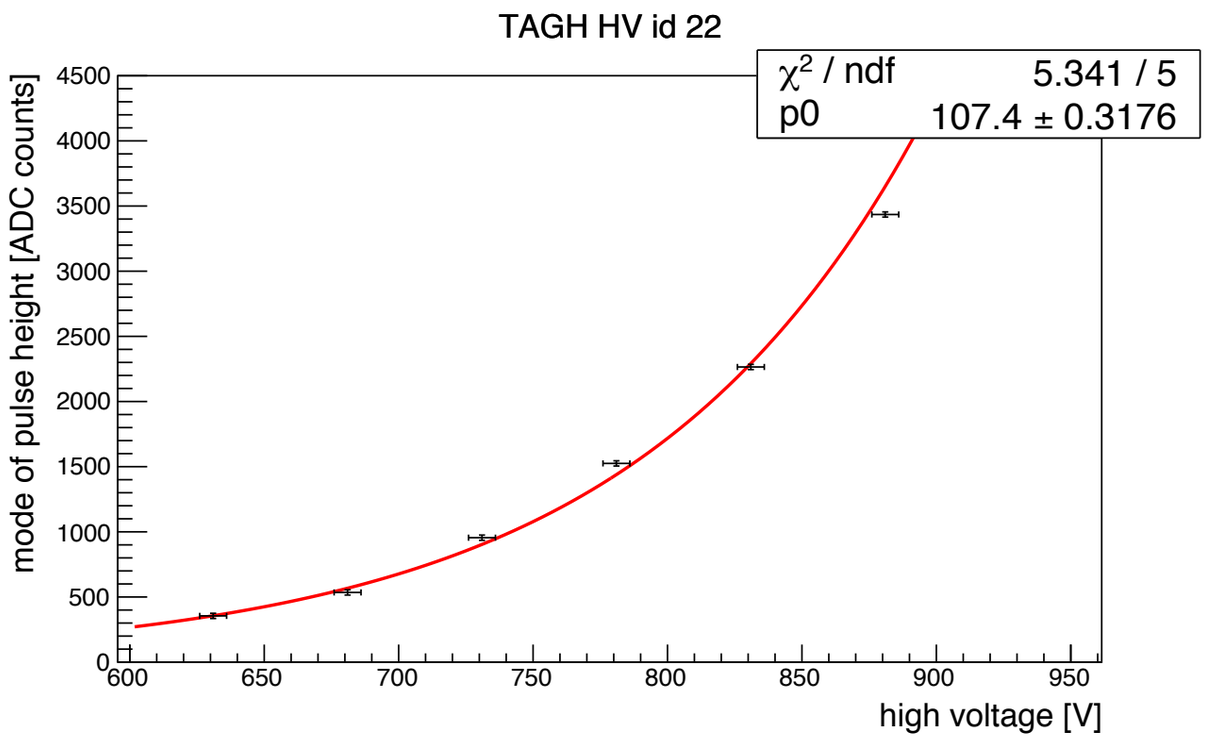
100 nA, PS_m7 trigger, 1e-3 RL converter

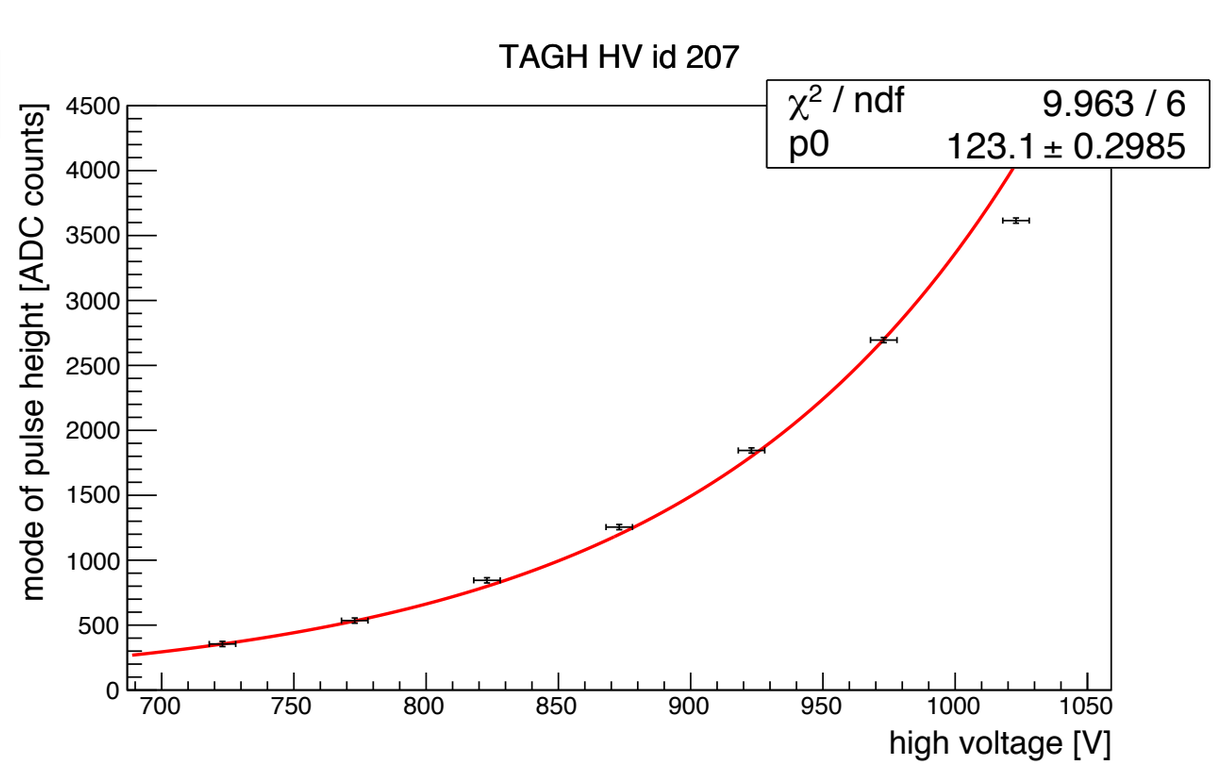
Run #	HV setting	Length	Events	Radiator
4168	initial	0:42:19	677k	2e-5 RL
4172	[] - 100 V	0:23:29	627k	1e-4 RL
4173	[] - 50 V	0:15:42	525k	1e-4 RL
4174	[] - 150 V	0:20:29	602k	…
4175	[] + 50 V	0:20:04	659k	…
4177	[] + 100 V	0:11:17	278k	…
4178	[] + 150 V	0:15:27	430k	…

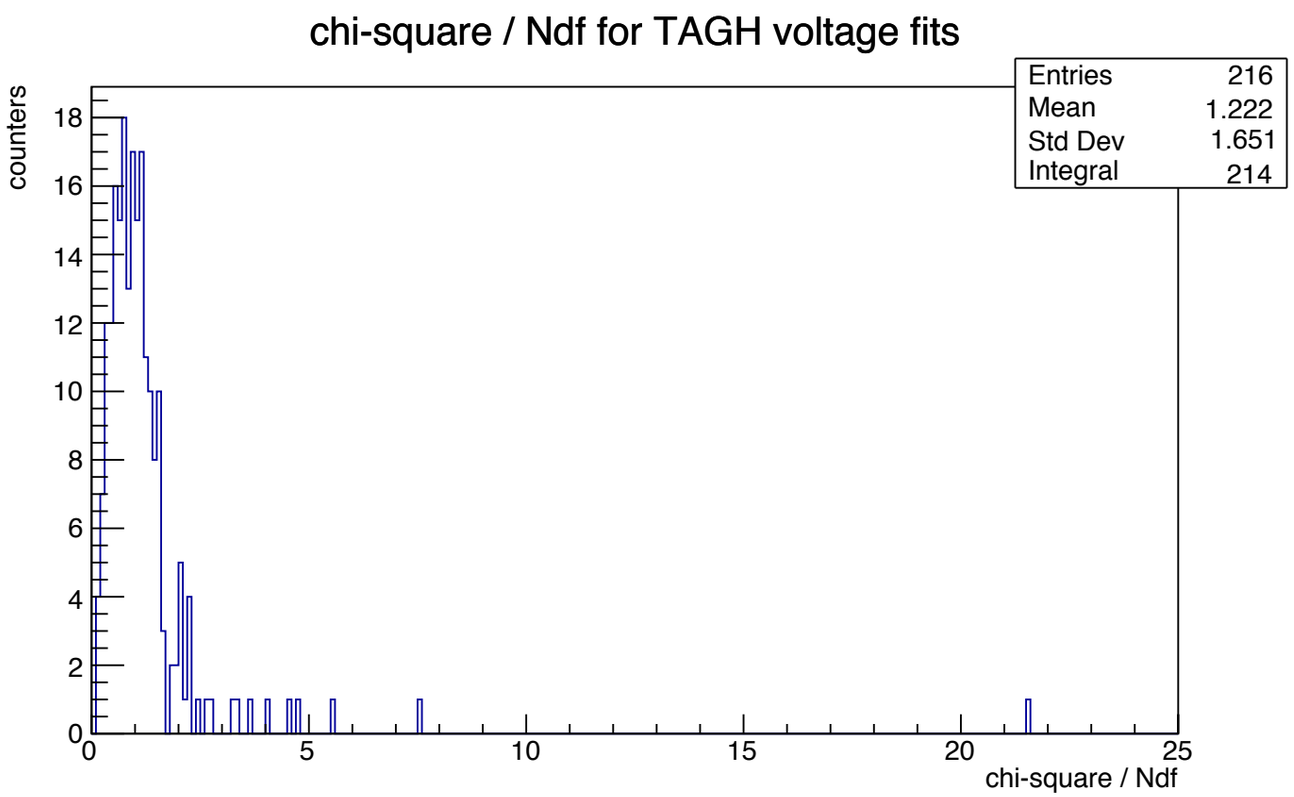
- Most pulses in runs 4177/4178 exceeded the 2V range of the ADCs

ADC pulse height

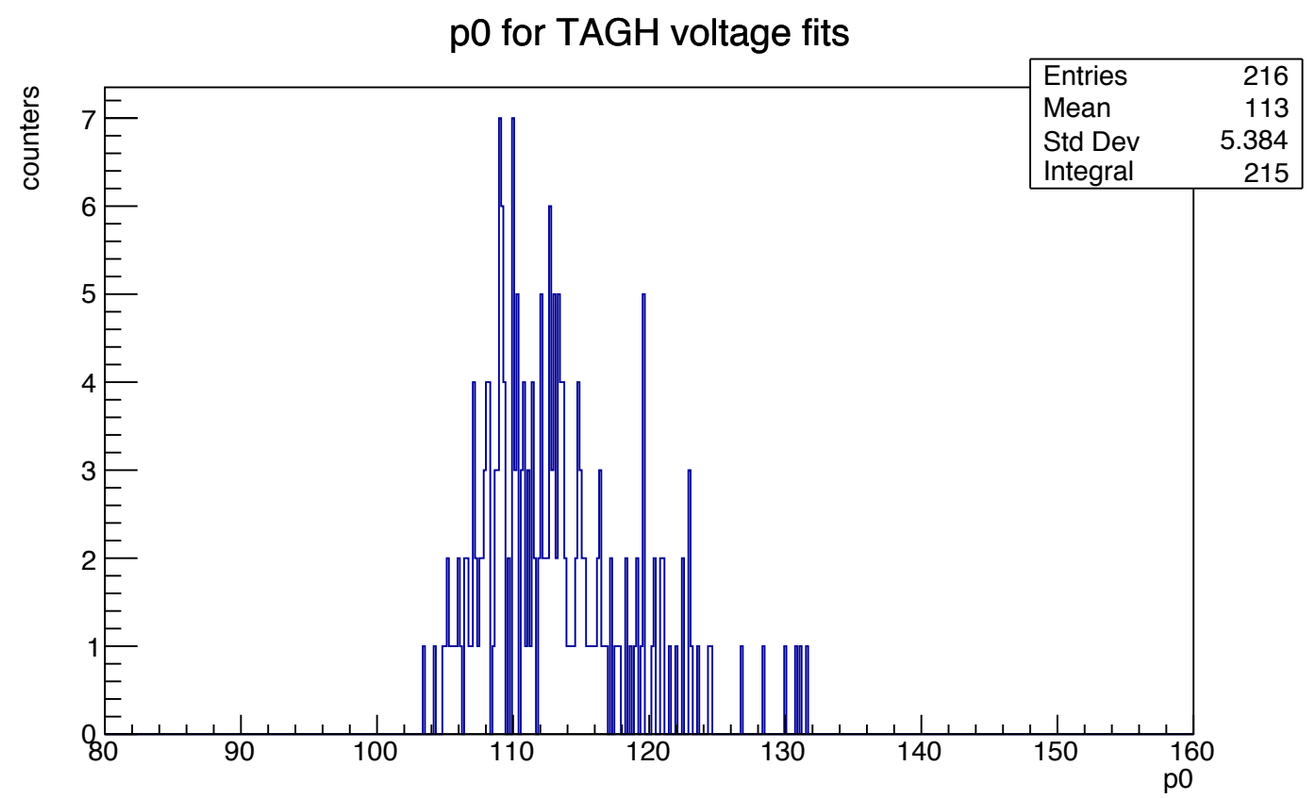
$$h(V) = \exp(V/p0)$$



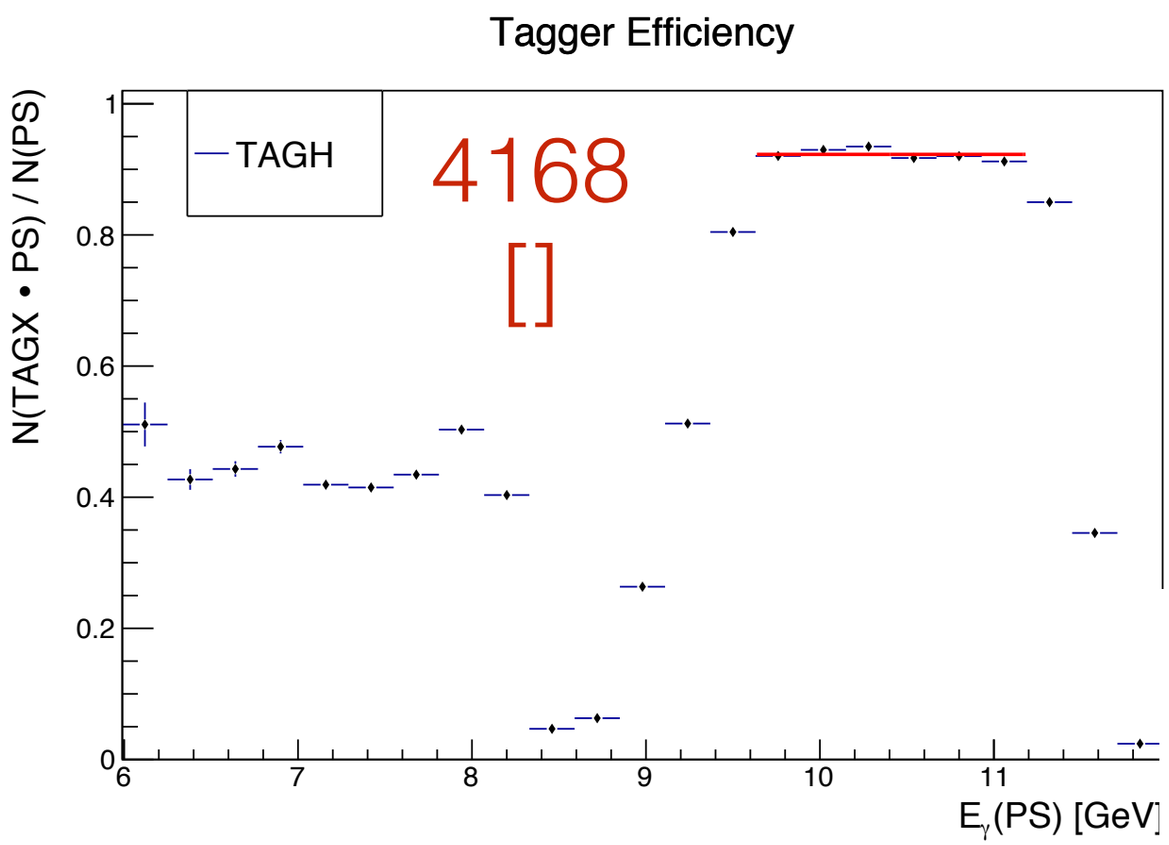


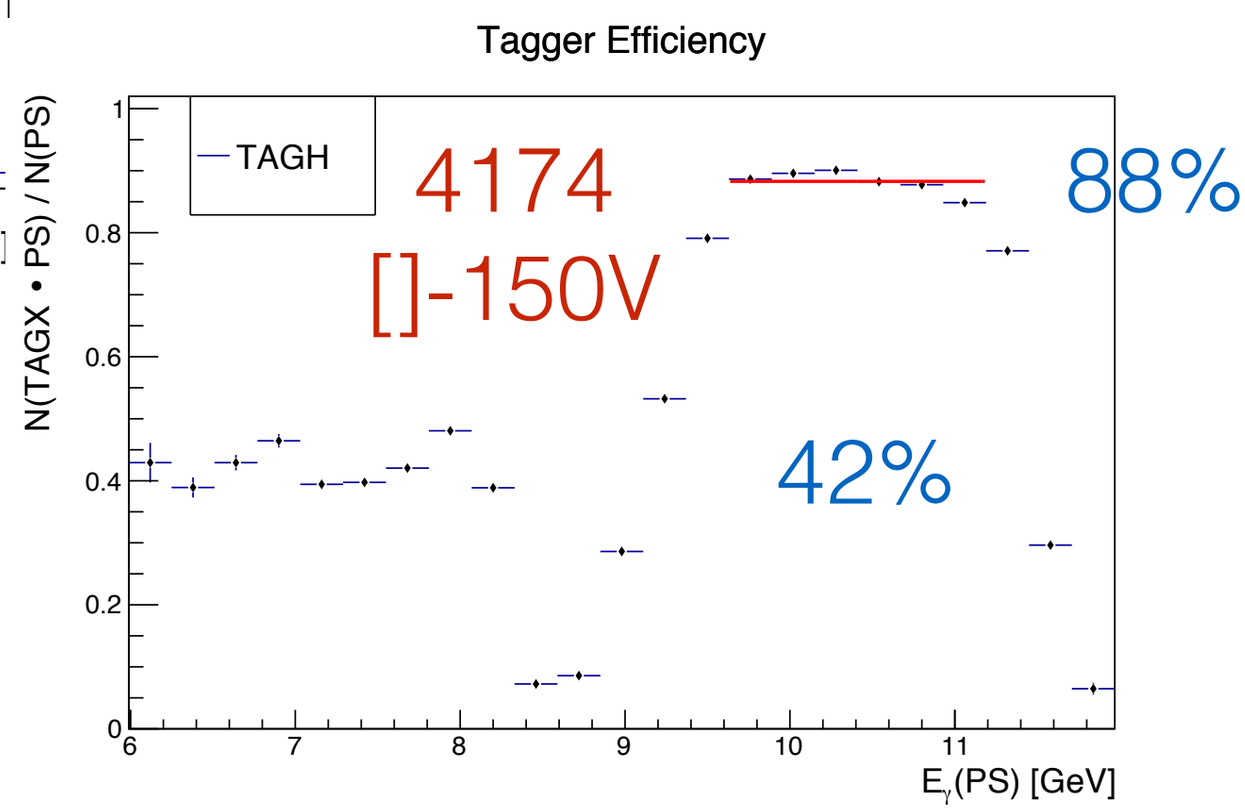


Pulse-Height Fit Results

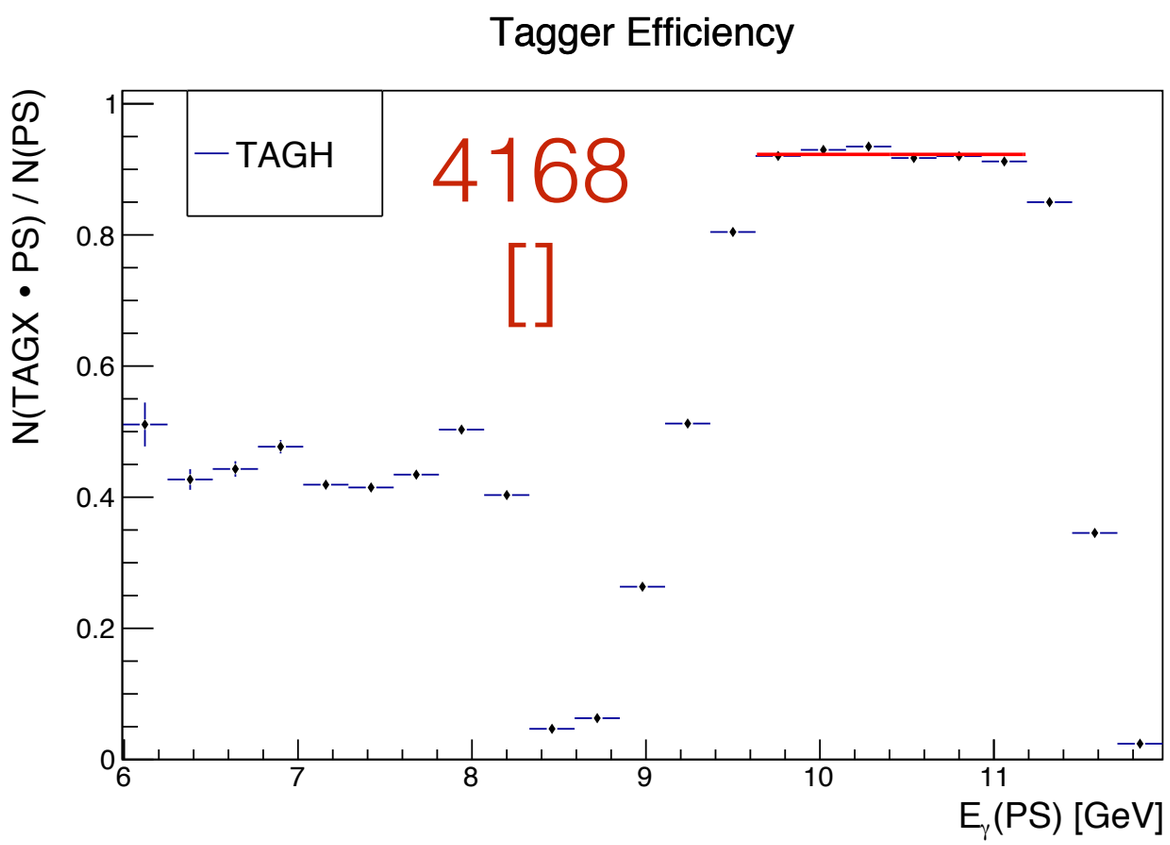


Tagger efficiency I



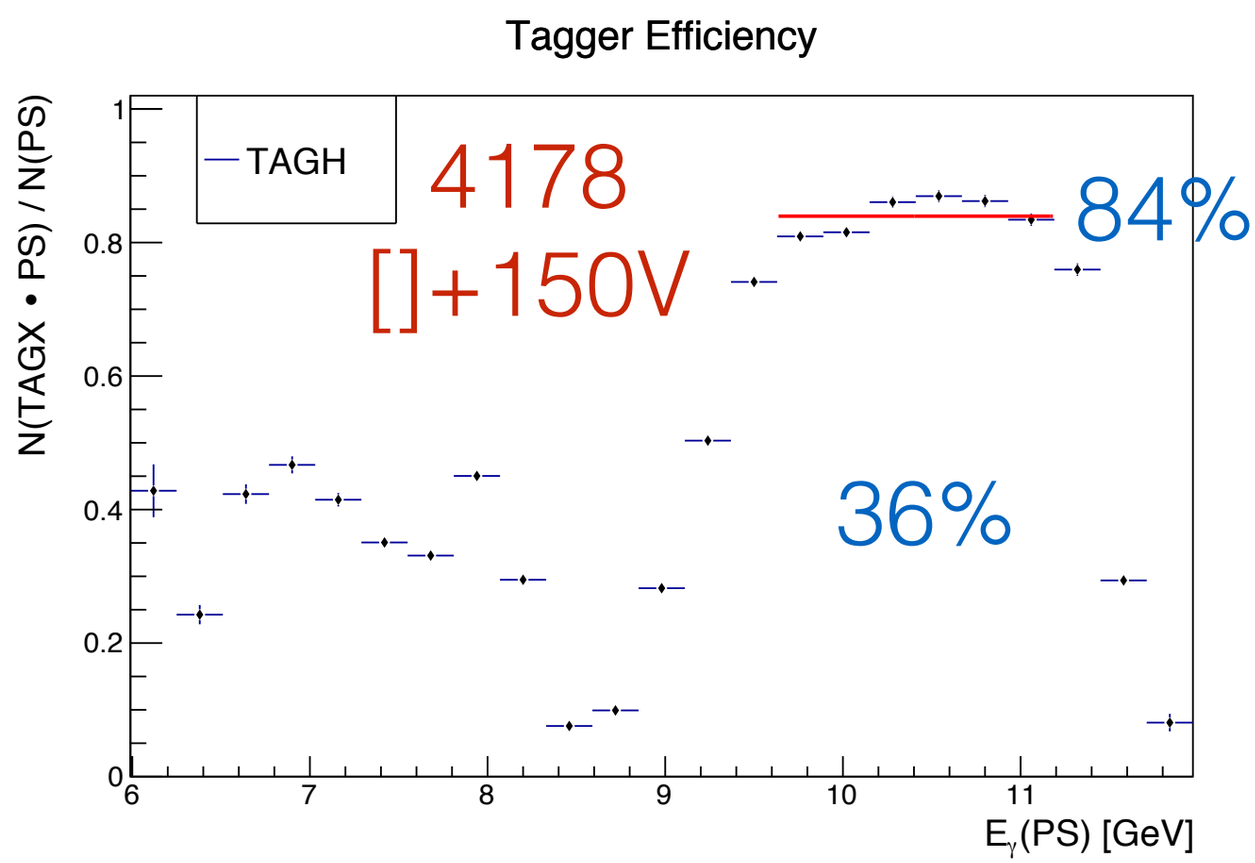


Tagger efficiency II

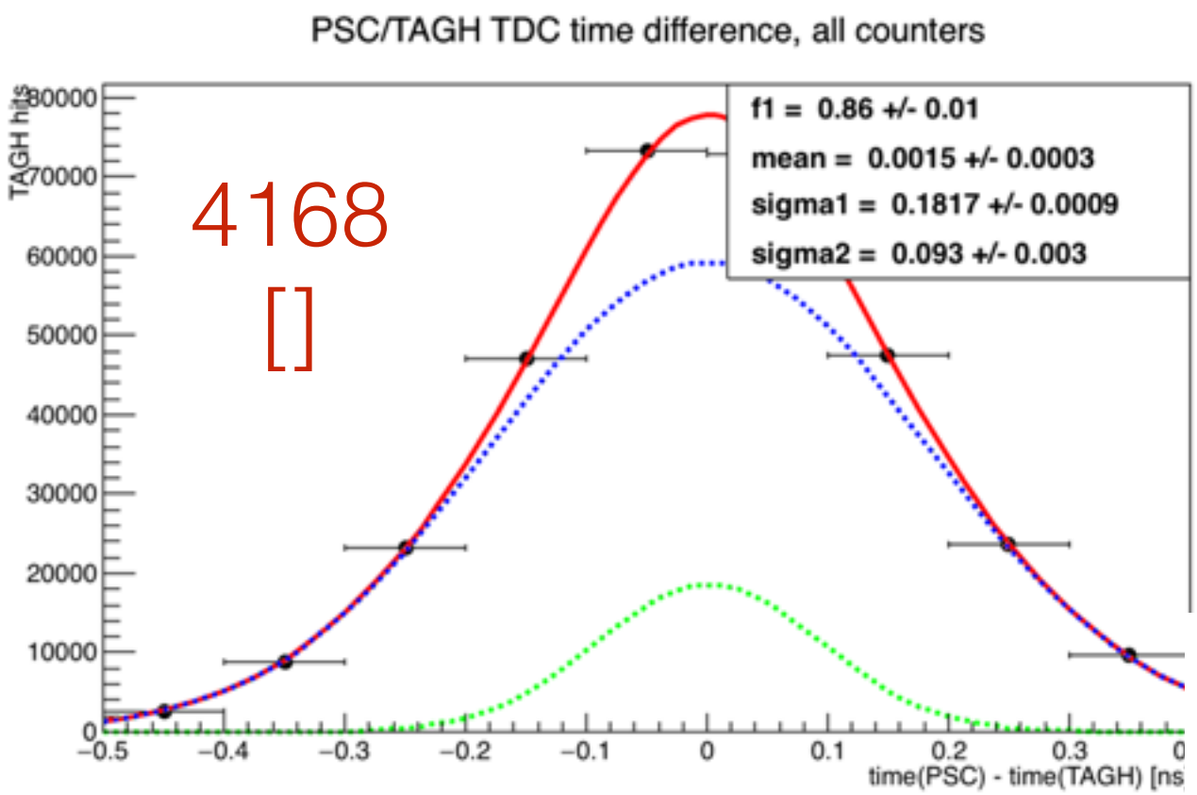


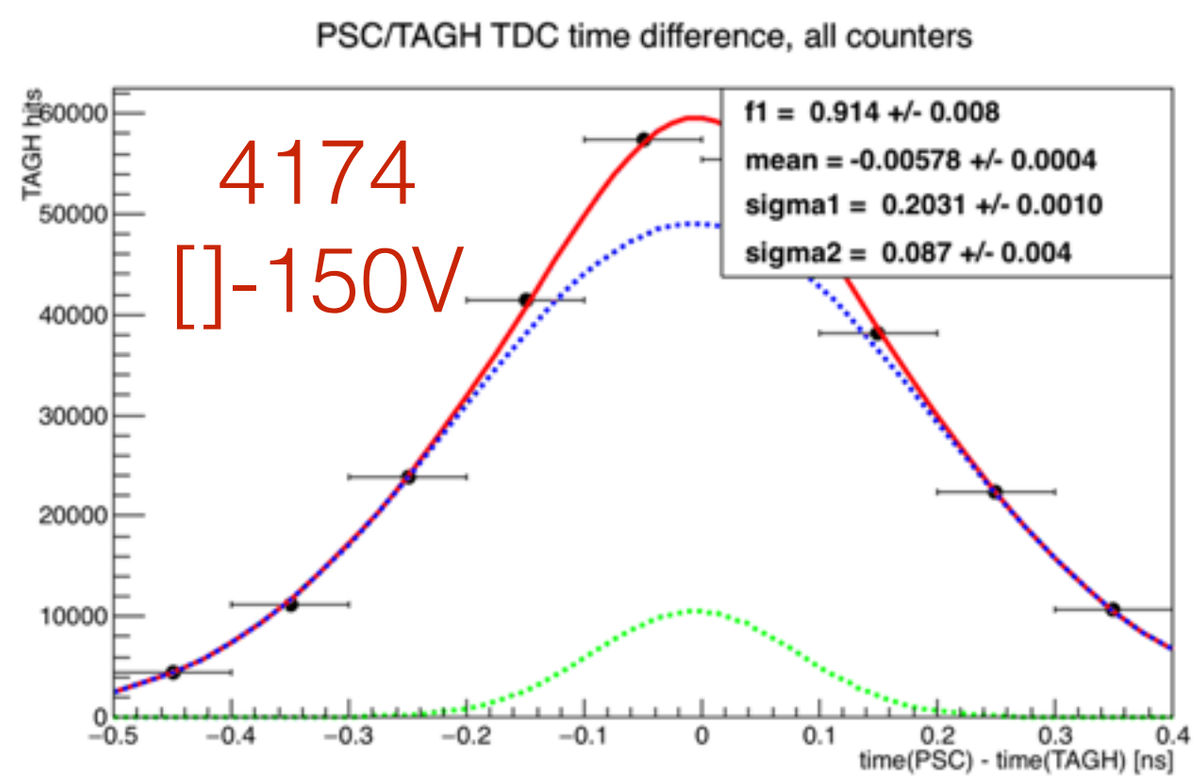
92%

44%



Timing resolution





s: combined sigma

s = sqrt(f1*s1^2+(1-f1)*s2^2))

Efficiencies and Timing Resolutions

d.s.: downstream u.s.: upstream

Run #	HV setting	d.s. eff.	u.s. eff.	sigma (ps)
4168	initial	44%	92%	172
4172	[] - 100 V	42%	90%	186
4173	[] - 50 V	43%	90%	184
4174	[] - 150 V	42%	88%	196
4175	[] + 50 V	43%	87%	191
4177	[] + 100 V	44%	84%	187
4178	[] + 150 V	36%	84%	201