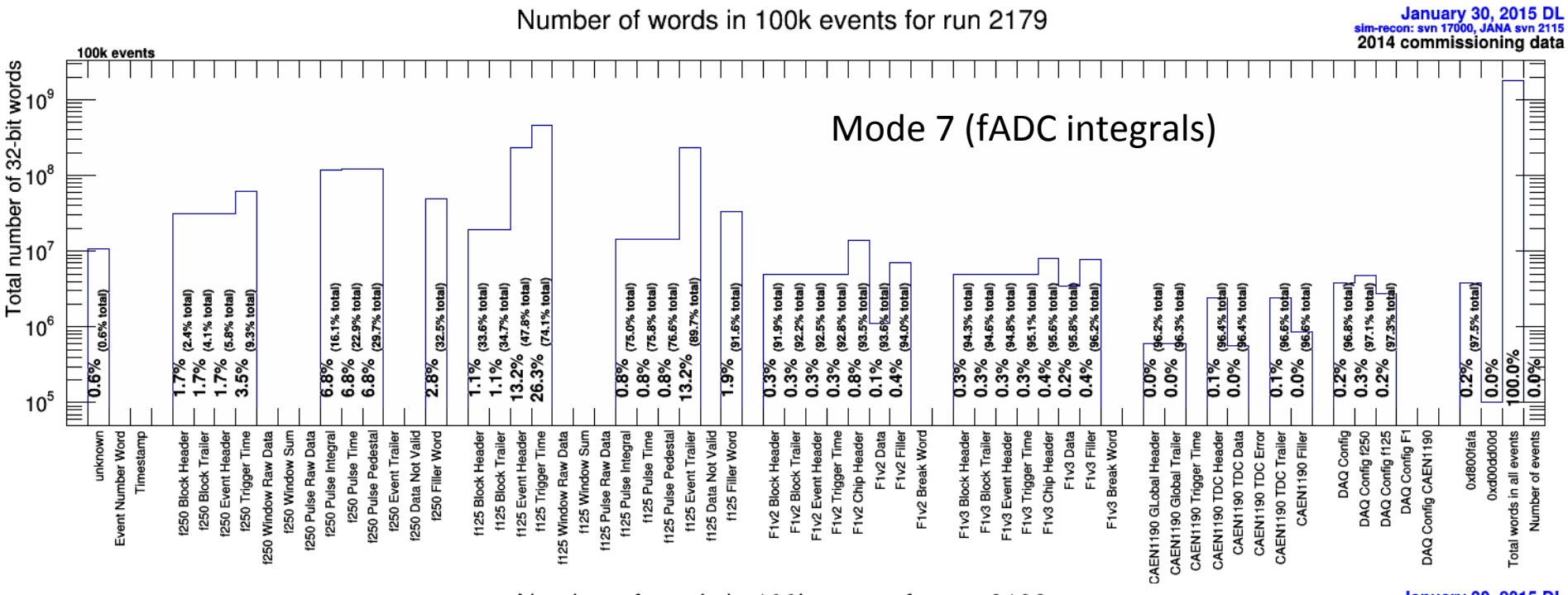
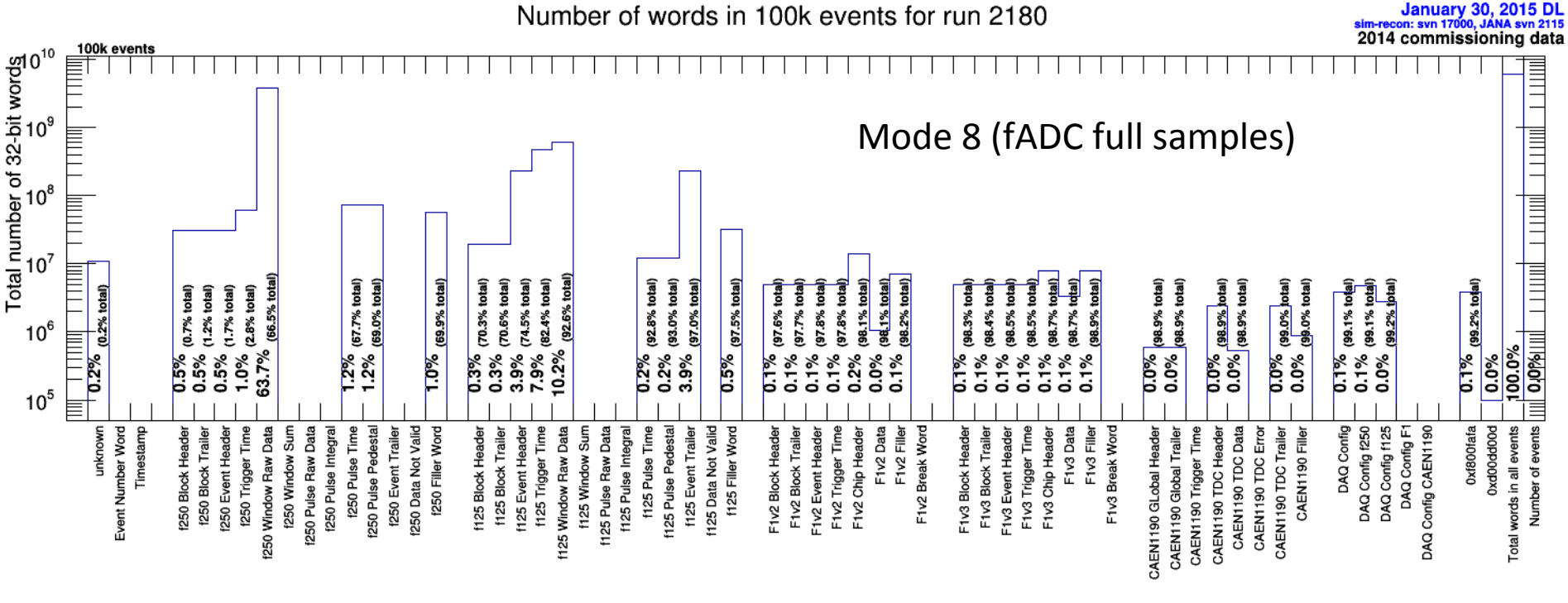
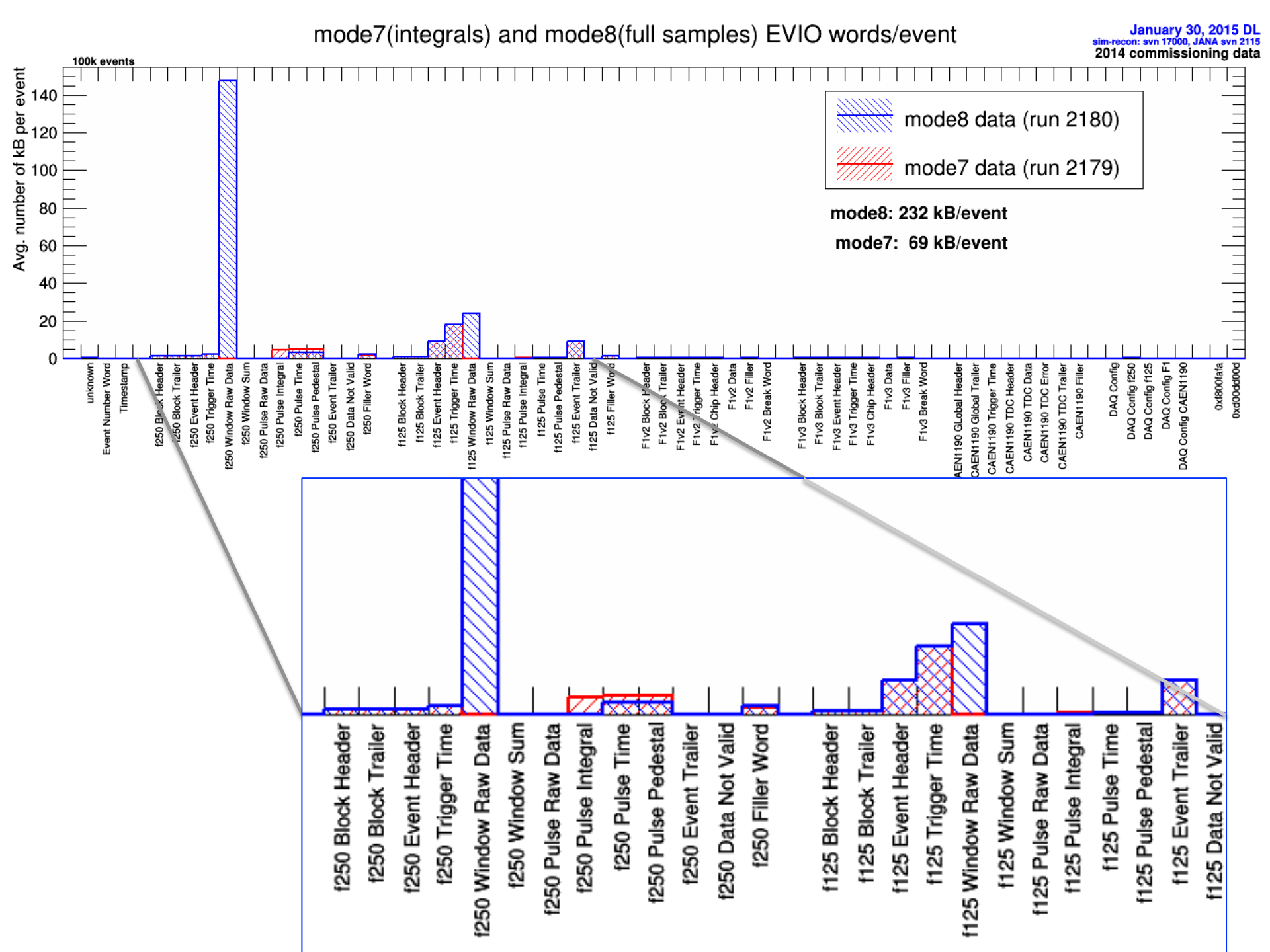
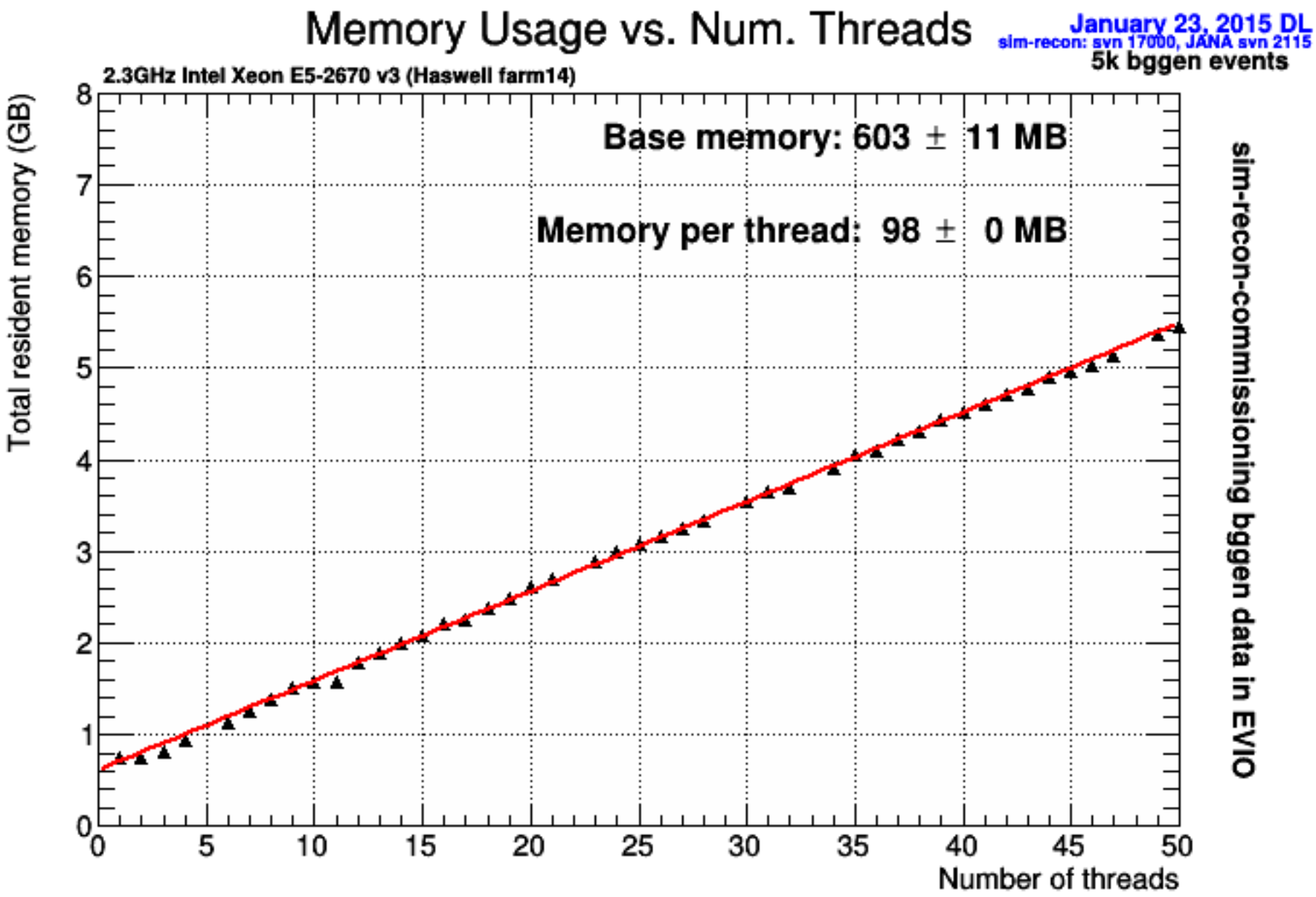
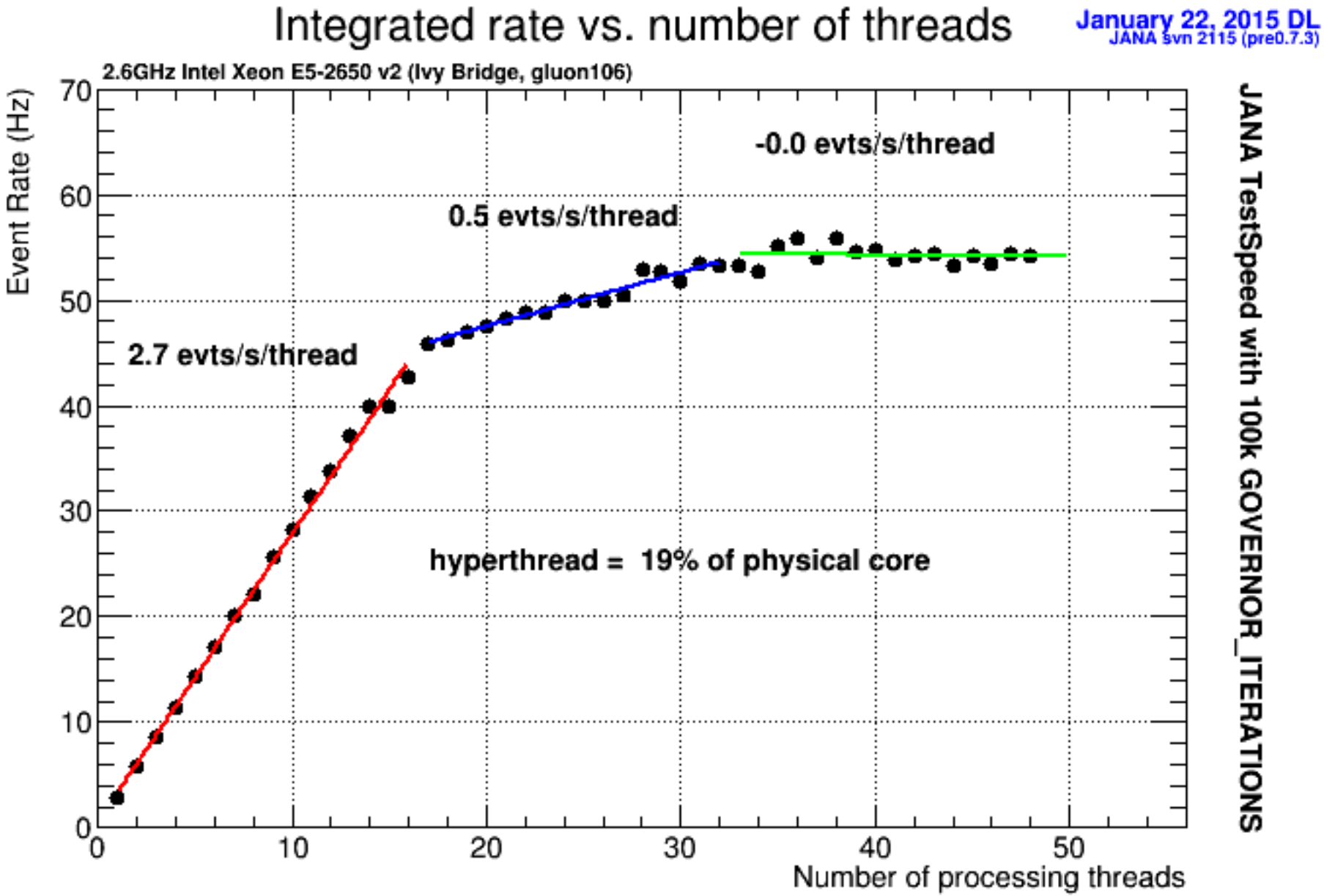
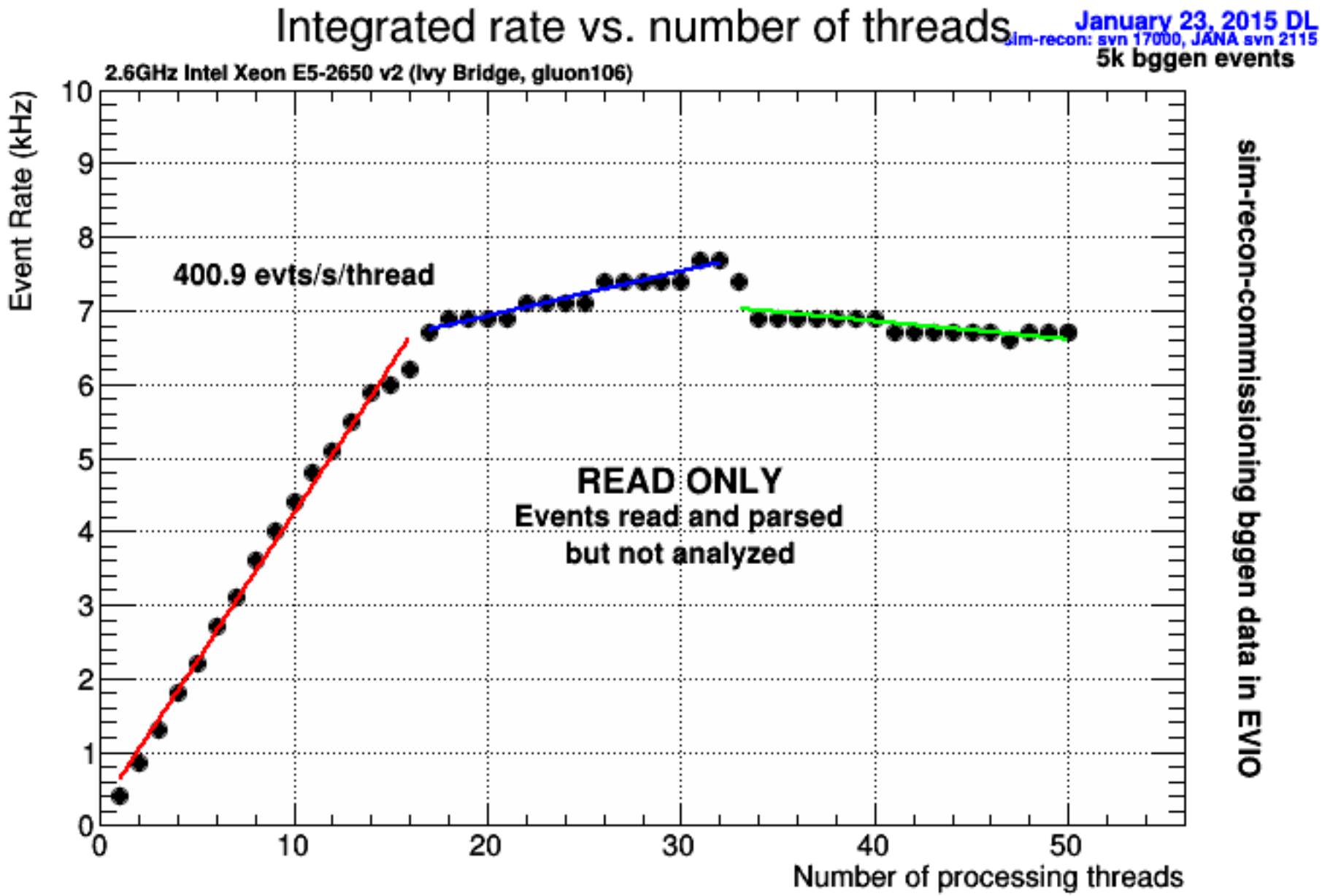

Number of words in 100k events for run 2179
January 30, 2015 DL
sim-recon: svn 17000, JANA svn 2115
2014 commissioning data
100k events
Mode 7 (fADC integrals)
Total number of 32-bit words
unknown
Event Number Word
Timestamp
f250 Block Header
f250 Block Trailer
f250 Event Header
f250 Trigger Time
f250 Window Raw Data
f250 Window Sum
f250 Pulse Raw Data
f250 Pulse Integral
f250 Pulse Time
f250 Pulse Pedestal
f250 Event Trailer
f250 Data Not Valid
f250 Filler Word
f125 Block Header
f125 Block Trailer
f125 Event Header
f125 Trigger Time
f125 Window Raw Data
f125 Window Sum
f125 Pulse Raw Data
f125 Pulse Integral
f125 Pulse Time
f125 Pulse Pedestal
f125 Event Trailer
f125 Data Not Valid
f125 Filler Word
F1v2 Block Header
F1v2 Block Trailer
F1v2 Event Header
F1v2 Trigger Time
F1v2 Chip Header
F1v2 Data
F1v2 Filler
F1v2 Break Word
F1v3 Block Header
F1v3 Block Trailer
F1v3 Event Header
F1v3 Trigger Time
F1v3 Chip Header
F1v3 Data
F1v3 Filler
F1v3 Break Word
CAEN1190 GLobal Header
CAEN1190 Global Trailer
CAEN1190 Trigger Time
CAEN1190 TDC Header
CAEN1190 TDC Data
CAEN1190 TDC Error
CAEN1190 TDC Trailer
CAEN1190 Filler
DAQ Config
DAQ Config f250
DAQ Config f125
DAQ Config F1
DAQ Config CAEN1190
0xf800fafa
0xd00dd00d
Total words in all events
Number of events

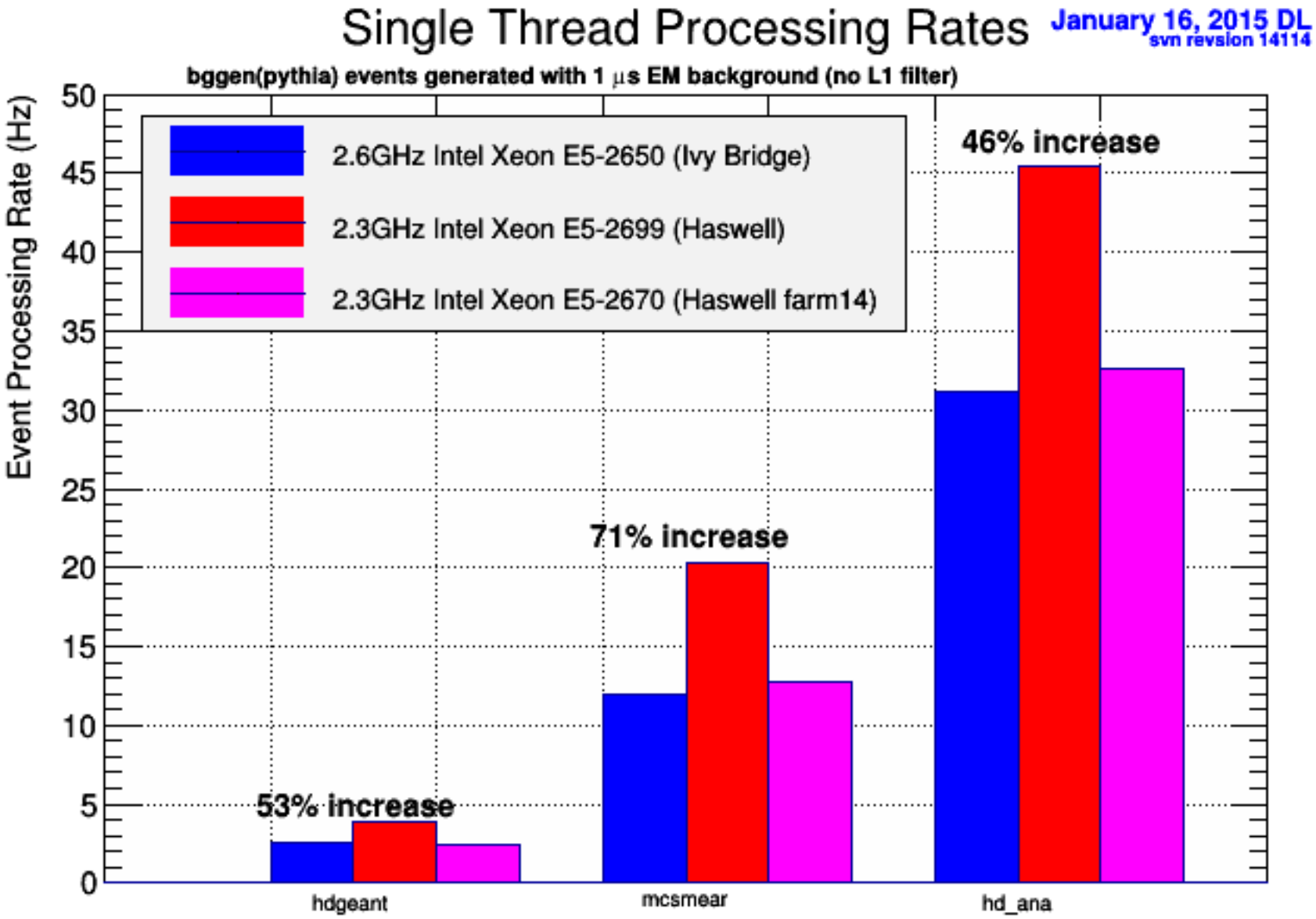

Number of words in 100k events for run 2180
January 30, 2015 DL
sim-recon: svn 17000, JANA svn 2115
2014 commissioning data
100k events
Mode 8 (fADC full samples)
Total number of 32-bit words
unknown
Event Number Word
Timestamp
f250 Block Header
f250 Block Trailer
f250 Event Header
f250 Trigger Time
f250 Window Raw Data
f250 Window Sum
f250 Pulse Raw Data
f250 Pulse Integral
f250 Pulse Time
f250 Pulse Pedestal
f250 Event Trailer
f250 Data Not Valid
f250 Filler Word
f125 Block Header
f125 Block Trailer
f125 Event Header
f125 Trigger Time
f125 Window Raw Data
f125 Window Sum
f125 Pulse Raw Data
f125 Pulse Integral
f125 Pulse Time
f125 Pulse Pedestal
f125 Event Trailer
f125 Data Not Valid
f125 Filler Word
F1v2 Block Header
F1v2 Block Trailer
F1v2 Event Header
F1v2 Trigger Time
F1v2 Chip Header
F1v2 Data
F1v2 Filler
F1v2 Break Word
F1v3 Block Header
F1v3 Block Trailer
F1v3 Event Header
F1v3 Trigger Time
F1v3 Chip Header
F1v3 Data
F1v3 Filler
F1v3 Break Word
CAEN1190 GLobal Header
CAEN1190 Global Trailer
CAEN1190 Trigger Time
CAEN1190 TDC Header
CAEN1190 TDC Data
CAEN1190 TDC Error
CAEN1190 TDC Trailer
CAEN1190 Filler
DAQ Config
DAQ Config f250
DAQ Config f125
DAQ Config F1
DAQ Config CAEN1190
0xf800fafa
0xd00dd00d
Total words in all events
Number of events

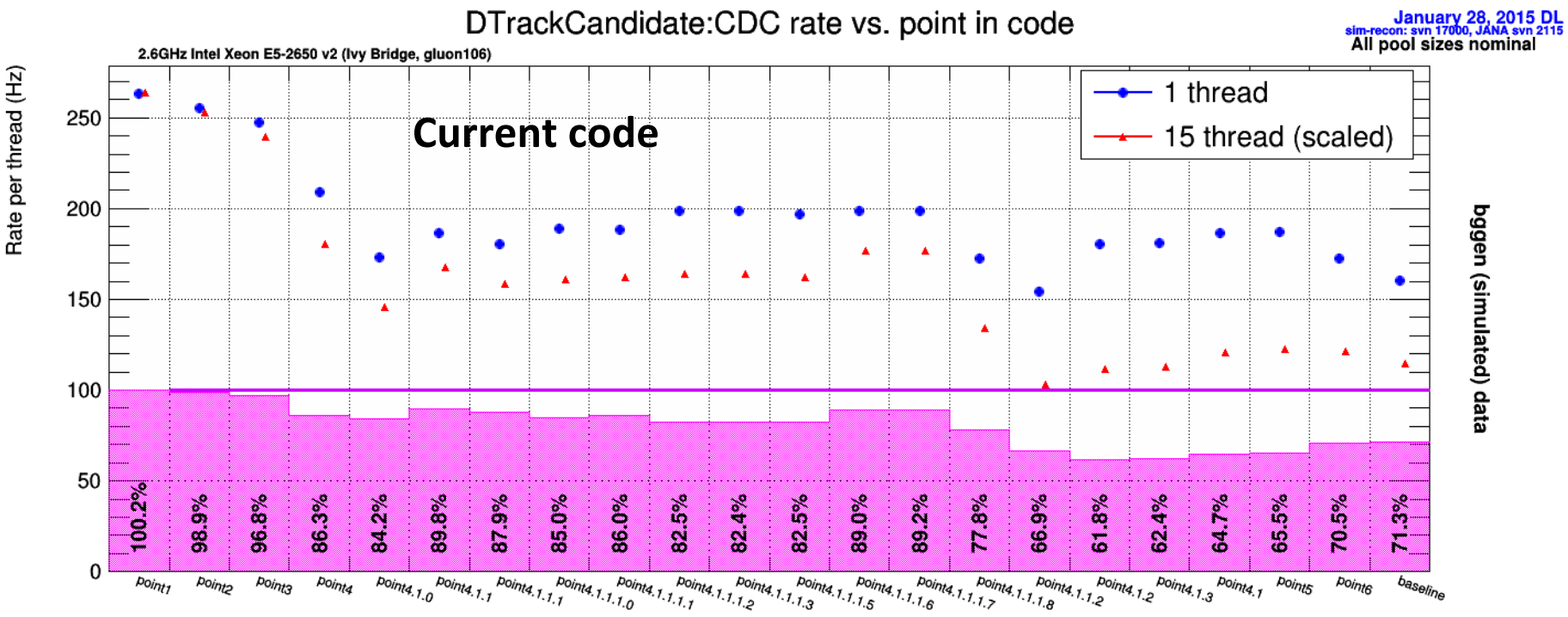

mode7(integrals) and mode8(full samples) EVIO words/event
January 30, 2015 DL
sim-recon: svn 17000, JANA svn 2115
2014 commissioning data
100k events
Avg. number of kB per event
mode8 data (run 2180)
mode7 data (run 2179)
mode8: 232 kB/event
mode7: 69 kB/event
unknown
Event Number Word
Timestamp
f250 Block Header
f250 Block Trailer
f250 Event Header
f250 Trigger Time
f250 Window Raw Data
f250 Window Sum
f250 Pulse Raw Data
f250 Pulse Integral
f250 Pulse Time
f250 Pulse Pedestal
f250 Event Trailer
f250 Data Not Valid
f250 Filler Word
f125 Block Header
f125 Block Trailer
f125 Event Header
f125 Trigger Time
f125 Window Raw Data
f125 Window Sum
f125 Pulse Raw Data
f125 Pulse Integral
f125 Pulse Time
f125 Pulse Pedestal
f125 Event Trailer
f125 Data Not Valid
f125 Filler Word
F1v2 Block Header
F1v2 Block Trailer
F1v2 Event Header
F1v2 Trigger Time
F1v2 Chip Header
F1v2 Data
F1v2 Filler
F1v2 Break Word
F1v3 Block Header
F1v3 Block Trailer
F1v3 Event Header
F1v3 Trigger Time
F1v3 Chip Header
F1v3 Data
F1v3 Filler
F1v3 Break Word
CAEN1190 GLobal Header
CAEN1190 Global Trailer
CAEN1190 Trigger Time
CAEN1190 TDC Header
CAEN1190 TDC Data
CAEN1190 TDC Error
CAEN1190 TDC Trailer
CAEN1190 Filler
DAQ Config
DAQ Config f250
DAQ Config f125
DAQ Config F1
DAQ Config CAEN1190
0xf800fafa
0xd00dd00d

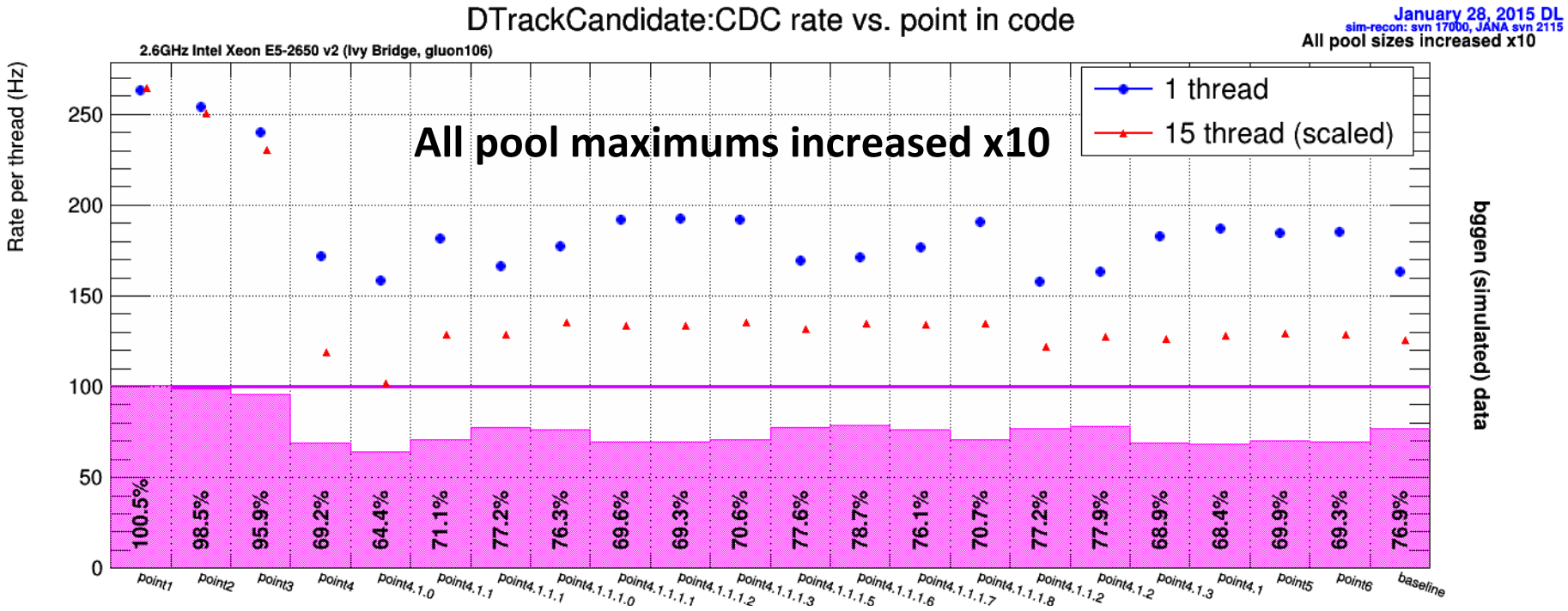

Memory Usage vs. Num. Threads
January 23, 2015 DL
sim-recon: svn 17000, JANA svn 2115
5k bggen events
2.3GHz Intel Xeon E5-2670 v3 (Haswell farm14)
Base memory: 603 ± 11 MB
Memory per thread: 98 ± 0 MB
Total resident memory (GB)
Number of threads
sim-recon-commissioning bggen data in EVIO
0
1
2
3
4
5
6
7
8
0
5
10
15
20
25
30
35
40
45
50

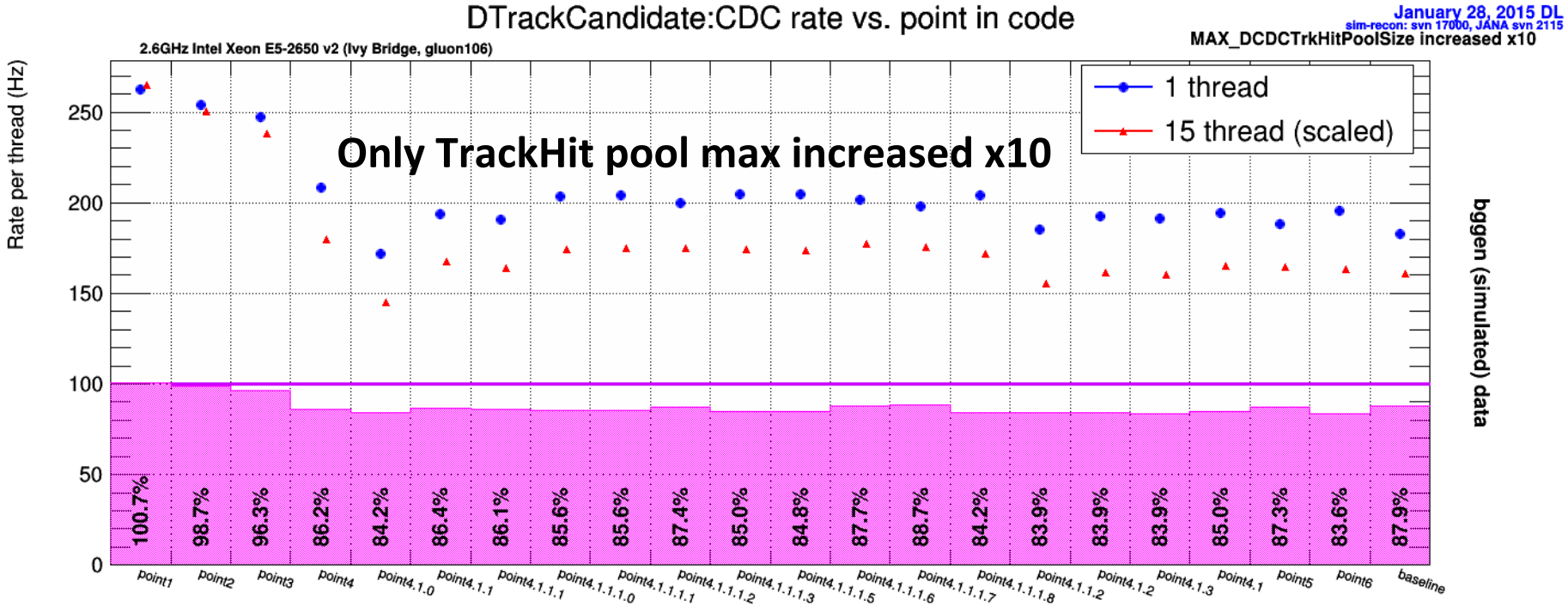

Integrated rate vs. number of threads
January 22, 2015 DL
JANA svn 2115 (pre0.7.3)
2.6GHz Intel Xeon E5-2650 v2 (Ivy Bridge, gluon106)
Event Rate (Hz)
Number of processing threads
-0.0 evts/s/thread
0.5 evts/s/thread
2.7 evts/s/thread
hyperthread = 19% of physical core
JANA TestSpeed with 100k GOVERNOR_ITERATIONS
0
10
20
30
40
50
60
70


Integrated rate vs. number of threads
January 23, 2015 DL
sim-recon: svn 17000, JANA svn 2115
5k bggen events
2.6GHz Intel Xeon E5-2650 v2 (Ivy Bridge, gluon106)
Event Rate (kHz)
400.9 evts/s/thread
READ ONLY
Events read and parsed
but not analyzed
Number of processing threads
sim-recon-commissioning bggen data in EVIO


Single Thread Processing Rates
January 16, 2015 DL
svn revsion 14114
bggen(pythia) events generated with 1 μs EM background (no L1 filter)
Event Processing Rate (Hz)
2.6GHz Intel Xeon E5-2650 (Ivy Bridge)
2.3GHz Intel Xeon E5-2699 (Haswell)
2.3GHz Intel Xeon E5-2670 (Haswell farm14)
53% increase
71% increase
46% increase
hdgeant
mcsmear
hd_ana


DTrackCandidate:CDC rate vs. point in code
January 28, 2015 DL
sim-recon: svn 17000, JANA svn 2115
All pool sizes nominal
2.6GHz Intel Xeon E5-2650 v2 (Ivy Bridge, gluon106)
Current code
1 thread
15 thread (scaled)
Rate per thread (Hz)
bggen (simulated) data
0
50
100
150
200
250
100.2%
98.9%
96.8%
86.3%
84.2%
89.8%
87.9%
85.0%
86.0%
82.5%
82.4%
82.5%
89.0%
89.2%
77.8%
66.9%
61.8%
62.4%
64.7%
65.5%
70.5%
71.3%
point1
point2
point3
point4
point4.1.0
point4.1.1
point4.1.1.1
point4.1.1.1.0
point4.1.1.1.1
point4.1.1.1.2
point4.1.1.1.3
point4.1.1.1.5
point4.1.1.1.6
point4.1.1.1.7
point4.1.1.1.8
point4.1.1.2
point4.1.2
point4.1.3
point4.1
point5
point6
baseline


DTrackCandidate:CDC rate vs. point in code
January 28, 2015 DL
sim-recon: svn 17000, JANA svn 2115
All pool sizes increased x10
2.6GHz Intel Xeon E5-2650 v2 (Ivy Bridge, gluon106)
All pool maximums increased x10
1 thread
15 thread (scaled)
Rate per thread (Hz)
bggen (simulated) data
100.5%
98.5%
95.9%
69.2%
64.4%
71.1%
77.2%
76.3%
69.6%
69.3%
70.6%
77.6%
78.7%
76.1%
70.7%
77.2%
77.9%
68.9%
68.4%
69.9%
69.3%
76.9%
point1
point2
point3
point4
point4.1.0
point4.1.1
point4.1.1.1
point4.1.1.1.0
point4.1.1.1.1
point4.1.1.1.2
point4.1.1.1.3
point4.1.1.1.5
point4.1.1.1.6
point4.1.1.1.7
point4.1.1.1.8
point4.1.1.2
point4.1.2
point4.1.3
point4.1
point5
point6
baseline


DTrackCandidate:CDC rate vs. point in code
January 28, 2015 DL
sim-recon: svn 17000, JANA svn 2115
MAX_DCDCTrkHitPoolSize increased x10
2.6GHz Intel Xeon E5-2650 v2 (Ivy Bridge, gluon106)
Only TrackHit pool max increased x10
1 thread
15 thread (scaled)
Rate per thread (Hz)
bggen (simulated) data
100.7%
98.7%
96.3%
86.2%
84.2%
86.4%
86.1%
85.6%
85.6%
87.4%
85.0%
84.8%
87.7%
88.7%
84.2%
83.9%
83.9%
83.9%
85.0%
87.3%
83.6%
87.9%
point1
point2
point3
point4
point4.1.0
point4.1.1
point4.1.1.1
point4.1.1.1.0
point4.1.1.1.1
point4.1.1.1.2
point4.1.1.1.3
point4.1.1.1.5
point4.1.1.1.6
point4.1.1.1.7
point4.1.1.1.8
point4.1.1.2
point4.1.2
point4.1.3
point4.1
point5
point6
baseline