72 Channel 125 MSPS ADC Status

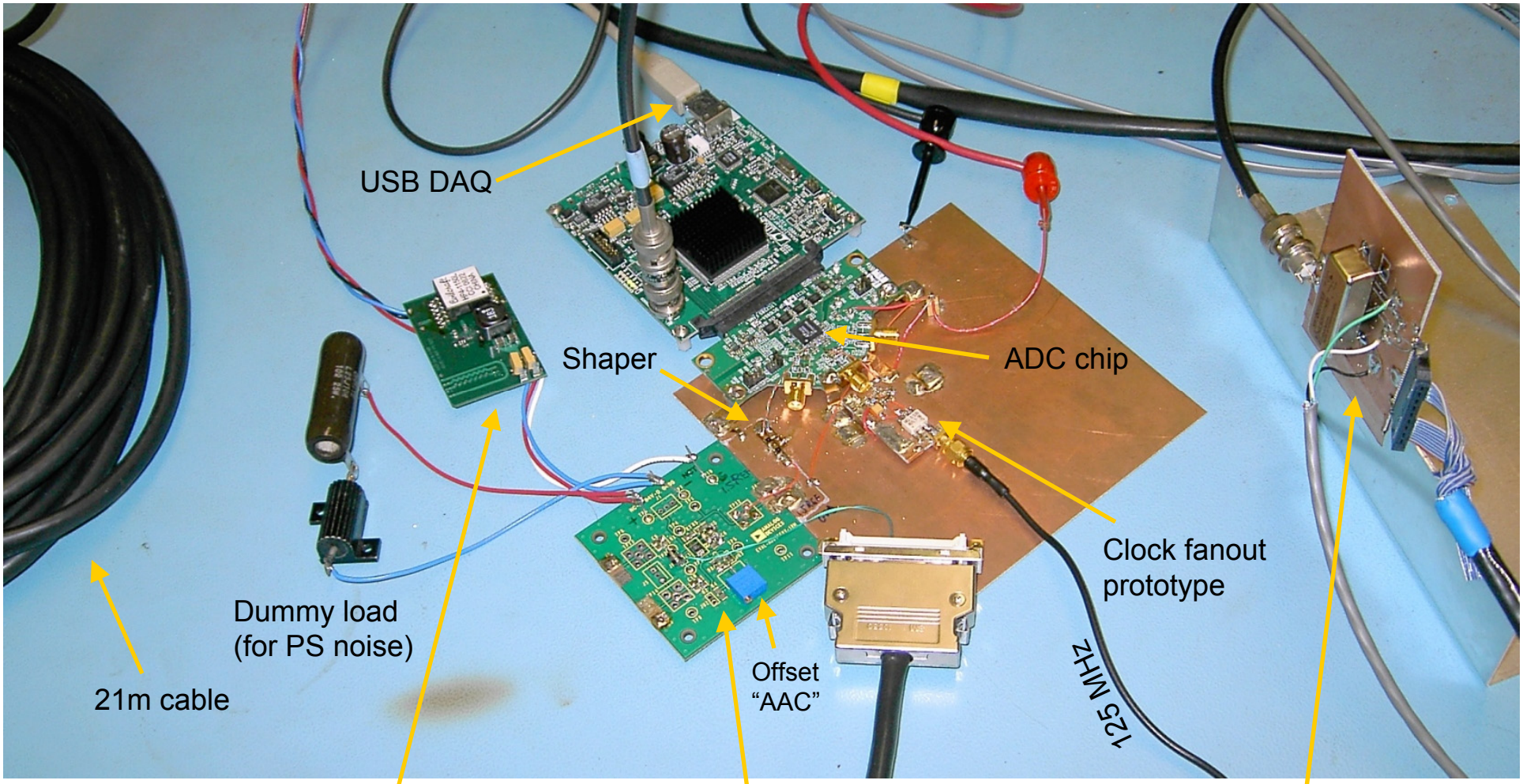
G. Visser

Indiana University Cyclotron Facility

8/22/2008

The development prototype (single channel)

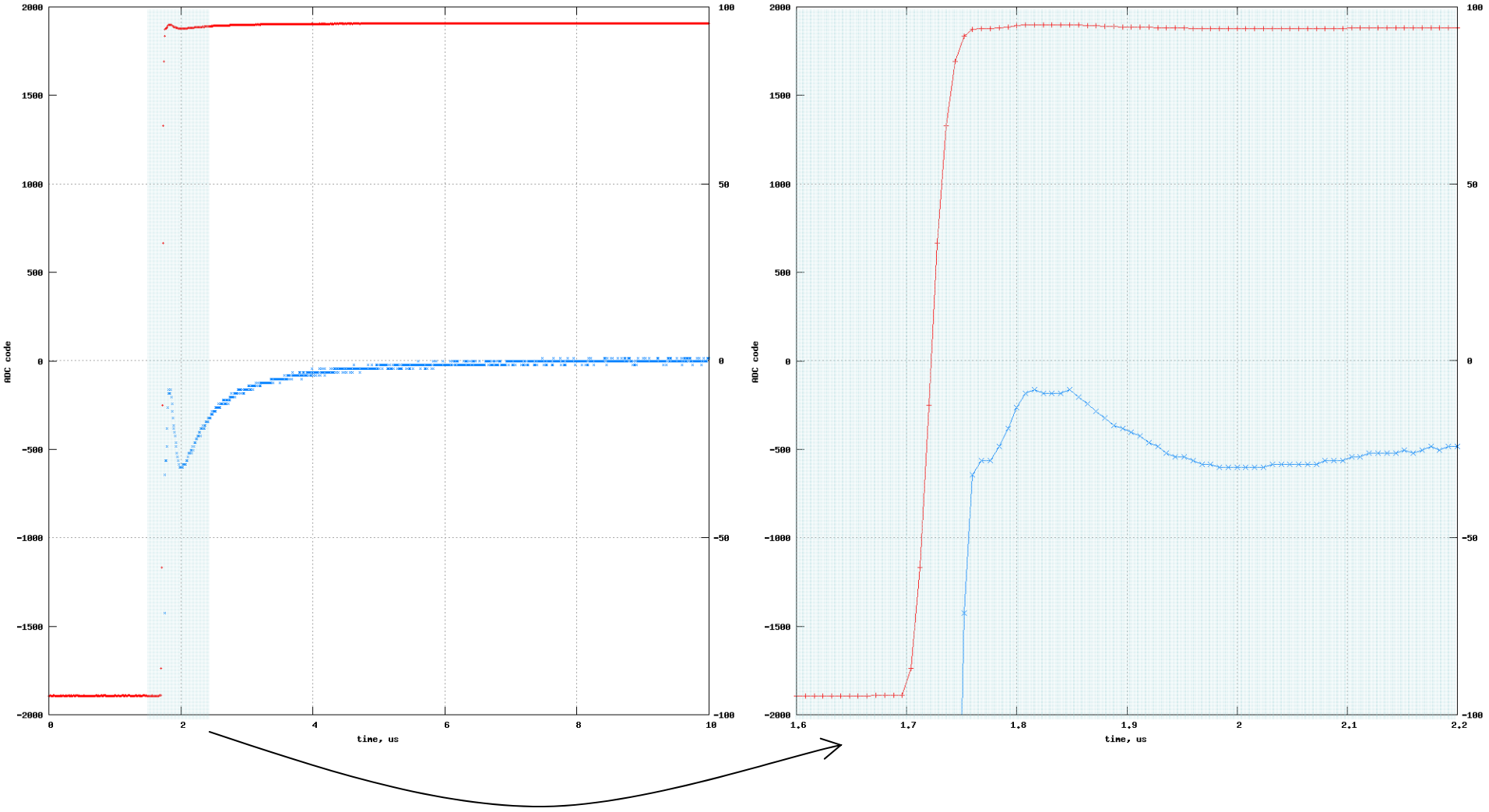
Presently has essentially the real implementation of line receiver, eq, shaper, ADC, clock fanout, PS for line receiver.
Missing: Offset DAC (not needed), ADC PS (should do), FPGA (not needed).



Step response of cable – ADC system

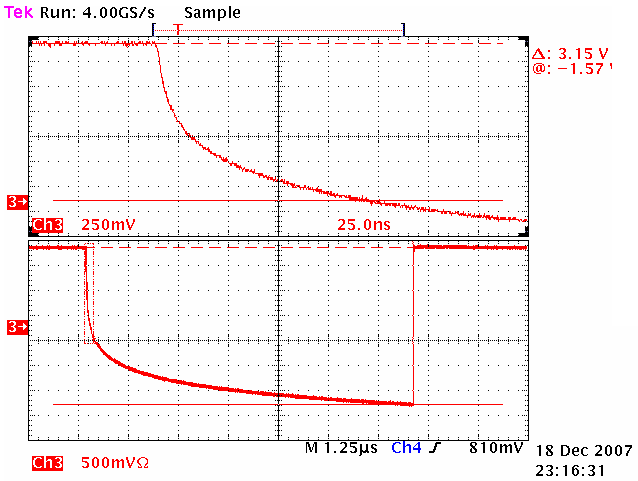
OUR GOAL: Provide a faithful measurement of ***the signal driven by the ASIC***, i.e., into terminated cable / ADC system

- Settles to <1% in 60 ns – if cable temperature is held within ± 5 °C
- Peaking time ≈ 28 ns for impulse input (about ½ the step risetime shown here)



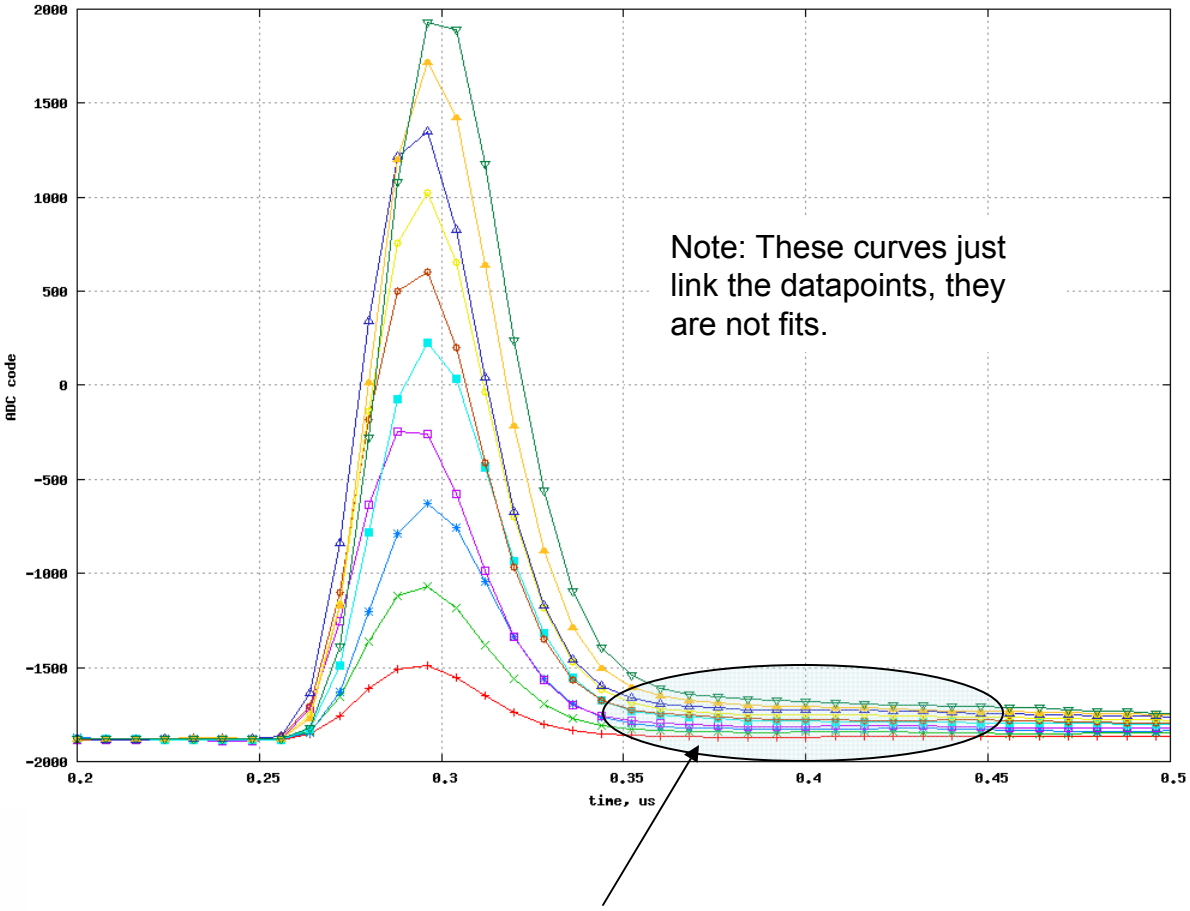
Detector-equivalent pulse response of ASIC – cable – ADC system

- Peaking time ≈ 30 ns
- Full width ≈ 90 ns at $^1/_{10}$ max
- Overall gain to pulse height ≈ 8.9 ADC units / electron
- Gain is a little less than present receiver/shaper feeding 1 Volt Struck ADC



Input test pulse to capacitor, as in GlueX-doc-931

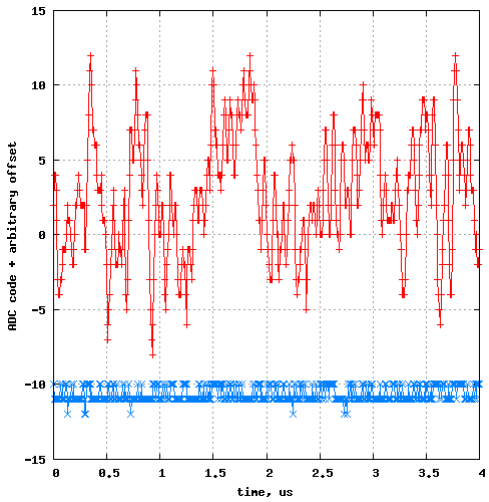
47 to 470 electrons, assuming 5×10^4 gain and t_0 = 1.38 ns



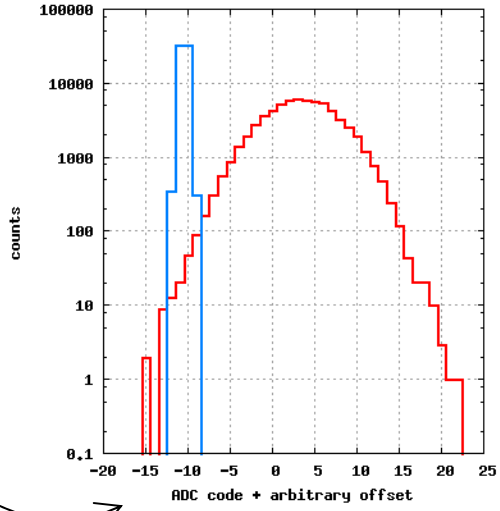
We could decide to adjust ADC equalization filter components (or use DSP) to better cancel the remaining tail. Decide it later, after some testing with detectors / GAS-2 / ADC. Remember, (PVC) cable temperature also affects the tail.

Noise

Time-domain noise, ASIC on/off

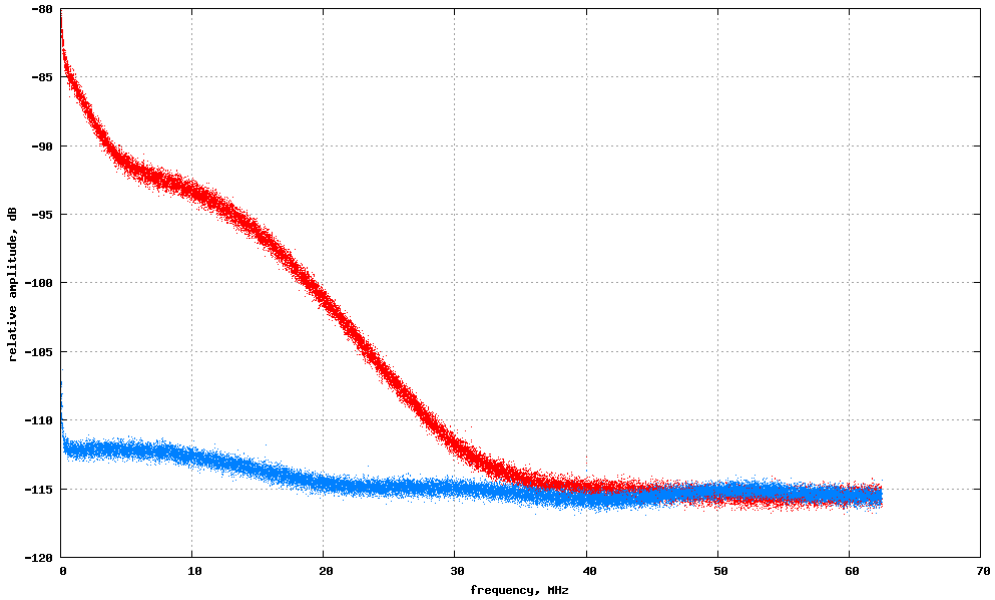


Noise histogram 64k consecutive samples, ASIC on/off



σ = 4.24
σ = 0.52

Noise power spectrum, 64k Hann window FFT, ASIC on/off

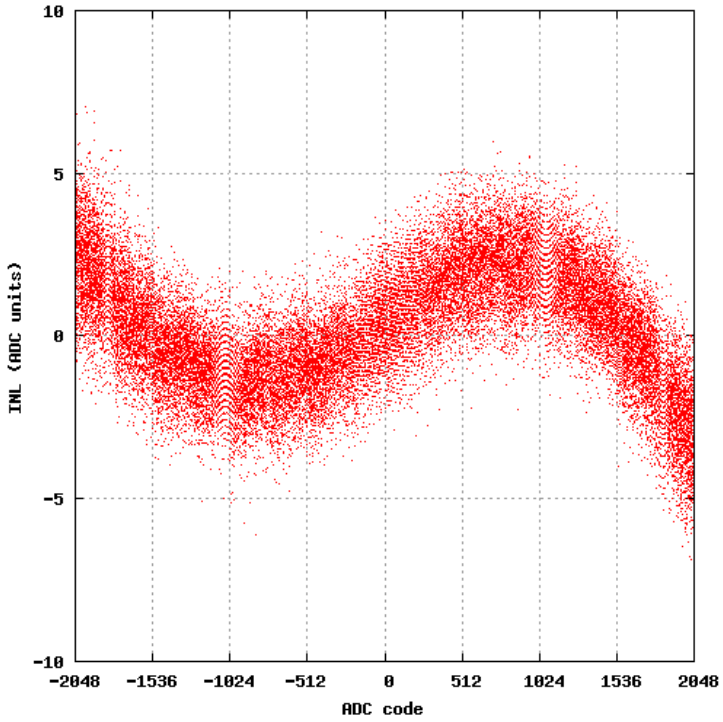


Conclusions

- Cable + ADC noise is negligible, even with gain set a little low as it is now
- Spectra look good, no spurious stuff such as PS ripple
- 12 bits is plenty! I don't see any justification for 14 bits, performance is not limited by ADC binning
- At 2pF detector capacitance, the ASIC *in this system* delivers effectively a noise σ ≈ 23,800 (total) electrons

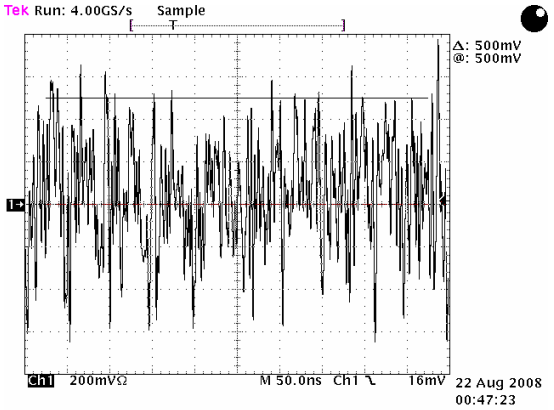
Linearity and Common-Mode Rejection

(Integral) linearity (from 500 kHz sine fit)

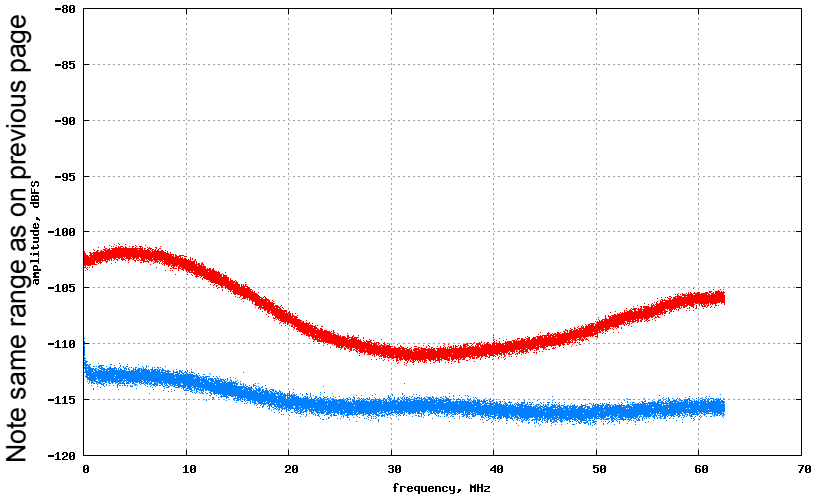


± 0.12%, mainly limited by AD8129 characteristics

Inject a harsh common-mode noise signal:



Noise w/ and w/out the common-mode noise signal



That much common-mode noise contributes only about as much as the ASIC noise with no detector capacitance – good!

What will be the production test plan?

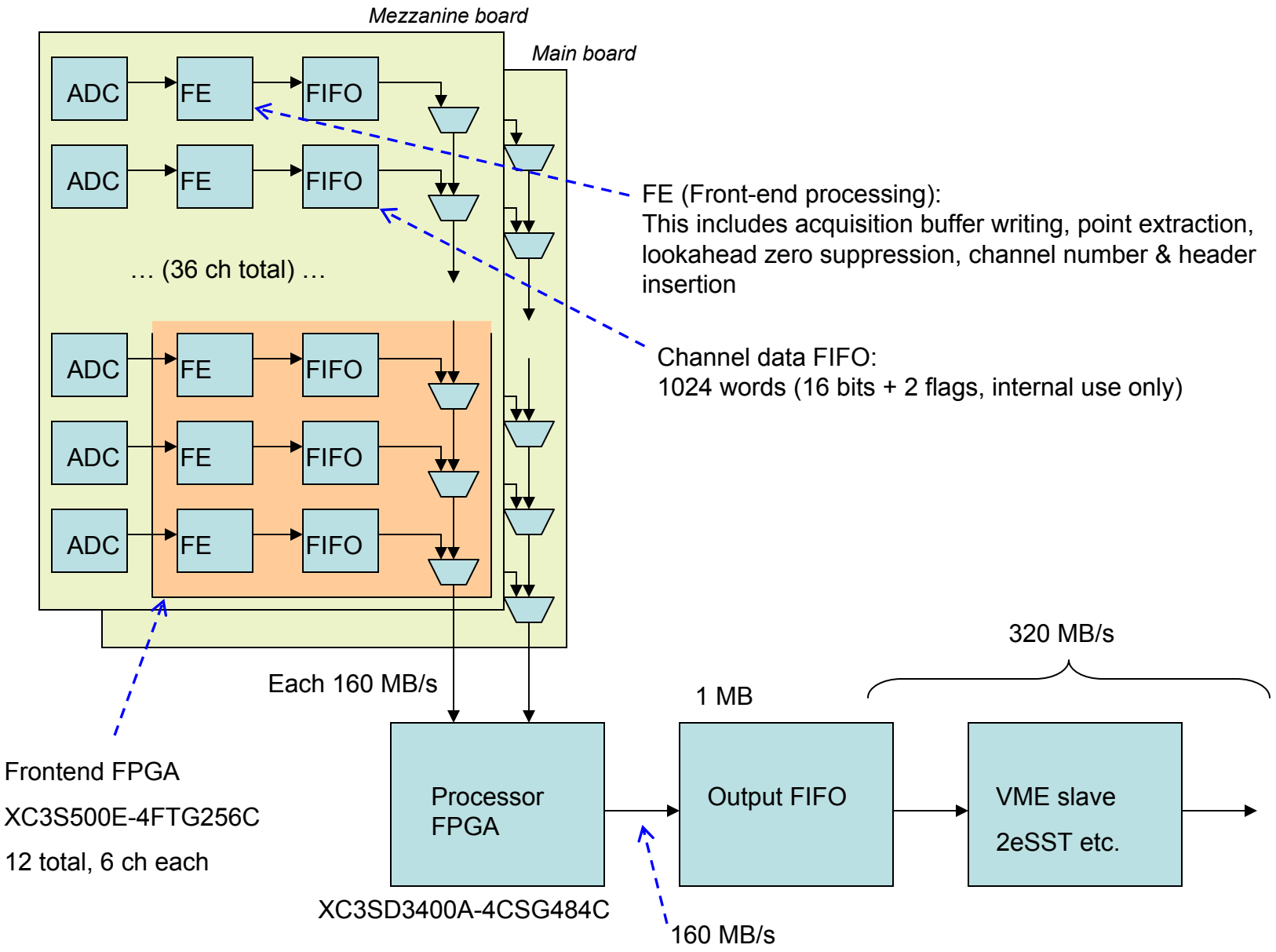
Some highlights:

- All supply voltages probed, input supply currents monitored (+5, +3.3, ±12 from backplane)
- DC transfer function (including linearity and missing-codes check), each channel, offset DAC → ADC
- Noise histogram, each channel
- Connect to input test fixture, standard pulse (step?) response check on each channel, synchronous to clock, i.e. tests also for clock problems.
- Data integrity checks from read/write test patterns and push test patterns to output FIFO

The above will be done at a semi-automated test station consisting of:

- VXS crate (JLab?) including CPU and trigger/clock source (VXS)
- Current monitor VME extender
- Perhaps an external computer to run the test software, at least something for operator interface
- Three plug-in test source modules, probably also involving a signal generator
- Benchtop DMM
- Other test equipment will of course be needed (and available) for diagnosis and repair…

Reminder / update on the ADC board datapath architecture



Status of the ADC125 design work

We were supposed to have a module by this time… Where is it?

- Input connectors and routing
- Line receiver / eq
- Offset DAC
- Shaper
- ADC
- ADC – FPGA routing
- FE FPGA readout daisy-chain
- FE FPGA pinout/symbol
- Line receiver PS
- Virtual ground / CM ref
- ADC analog PS
- Line receiver PS prototype
- ADC analog PS prototype
- Sample clock tree
- Clock / trig inputs P2 + VXS
- Clock / trig receiver
- Pulser (to detector)
- FE – Proc routing
- Proc – FIFO routing
- Proc FPGA pinout/symbol
- FIFO – VME FPGA routing
- VME FPGA – xcvr routing
- VME FPGA pinout/symbol
- P1/P2 routing
- +1.2V PS
- +2.5V PS
- Config flash
- JTAG routing
- Local clock distribution
- Full signal path prototype
- Thermal analysis
- Mezzanine stacking conn.
- Board materials & layer stack
- Power plane segmentation
- Silkscreen scrub
- Final channel copy/paste
- Main – mezzanine copy/paste
- ADC, FPGA procurement
- Misc. parts procurement
- Fabrication
- FE FPGA frontend
- FE FPGA backend / readout
- Proc FPGA datapath
- Proc FPGA trigger handling
- VME FPGA datapath
- VME FPGA controls
- VME FPGA configuration
- Programmer's reference manual
- Testing & evaluation
- ADC125 design report
- Delivery for FDC/CDC work

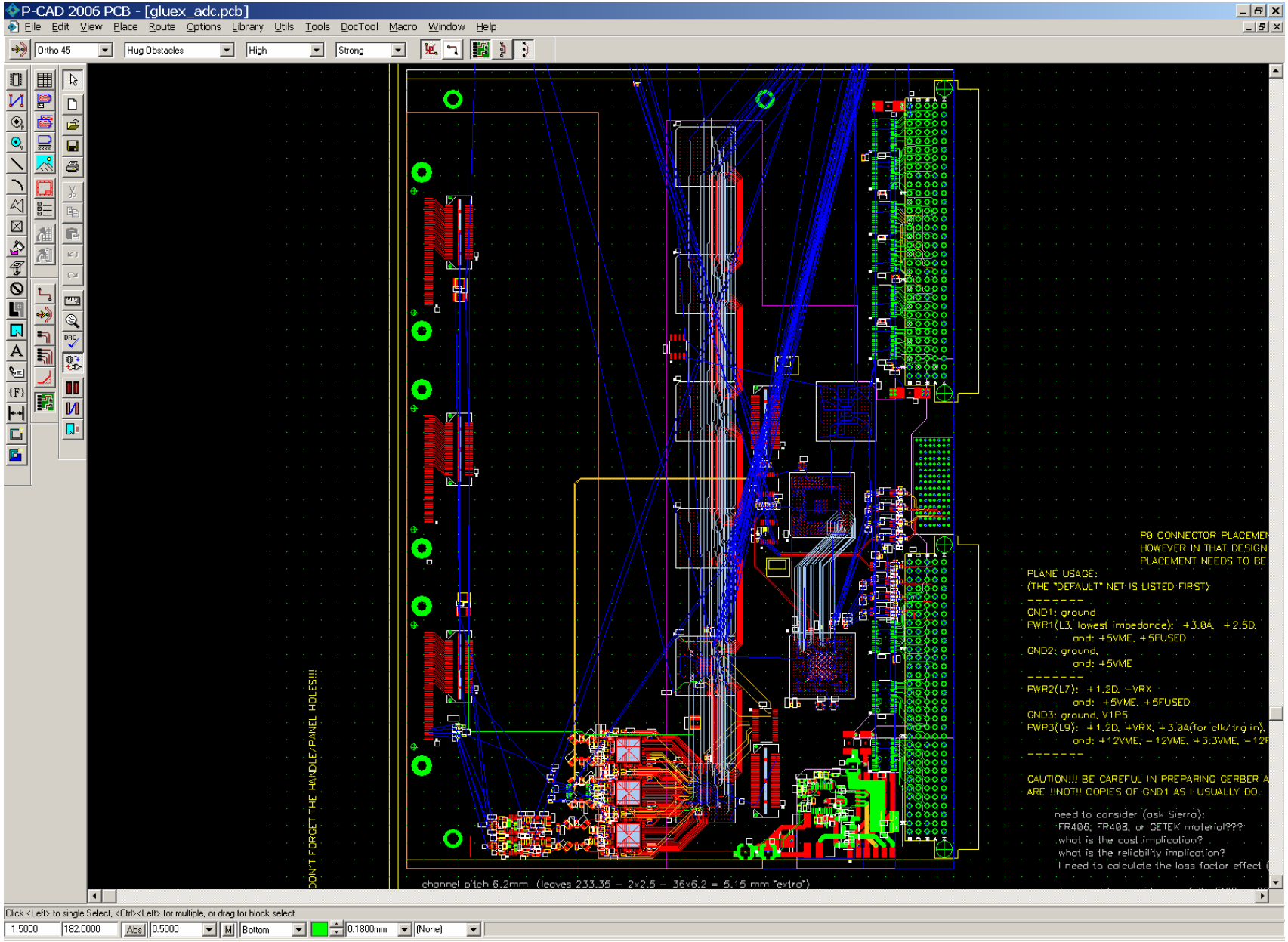
Green is done.

Blue are "final steps" to fabrication.

Underlined are the tasks I'm currently working on.

The mainboard layout today

Please note, it looks “empty” but there is a lot of trivial copy/past that will happen!



Contract status

It started about 10/7/2007 (according to my IUCF effort reporting)

As of this week:

• Labor 520 hours – 51% of budget (1015 hours)

• Materials $10,094 (including $6,791 for ADC chips) – 39 % of budget

Performance: Average (over whole period) time committed ≈ 32% – is 64% of planned

Recently, 104 / 185 hours

I can offer excuses from other projects, of course, but that is not all so helpful…

Billing status:

• Should have billed some time ago, but…

• IU accountants mistakenly applied overhead although it was supposed to be waived for this project as a capital construction effort…

• Then they realized it and have taken an inappropriately long time to fix it…

• Because of all that, they haven't yet sent a bill…

• I am told that one will be sent by about 9/8