



72 CHANNEL 125 MSPS ADC STATUS

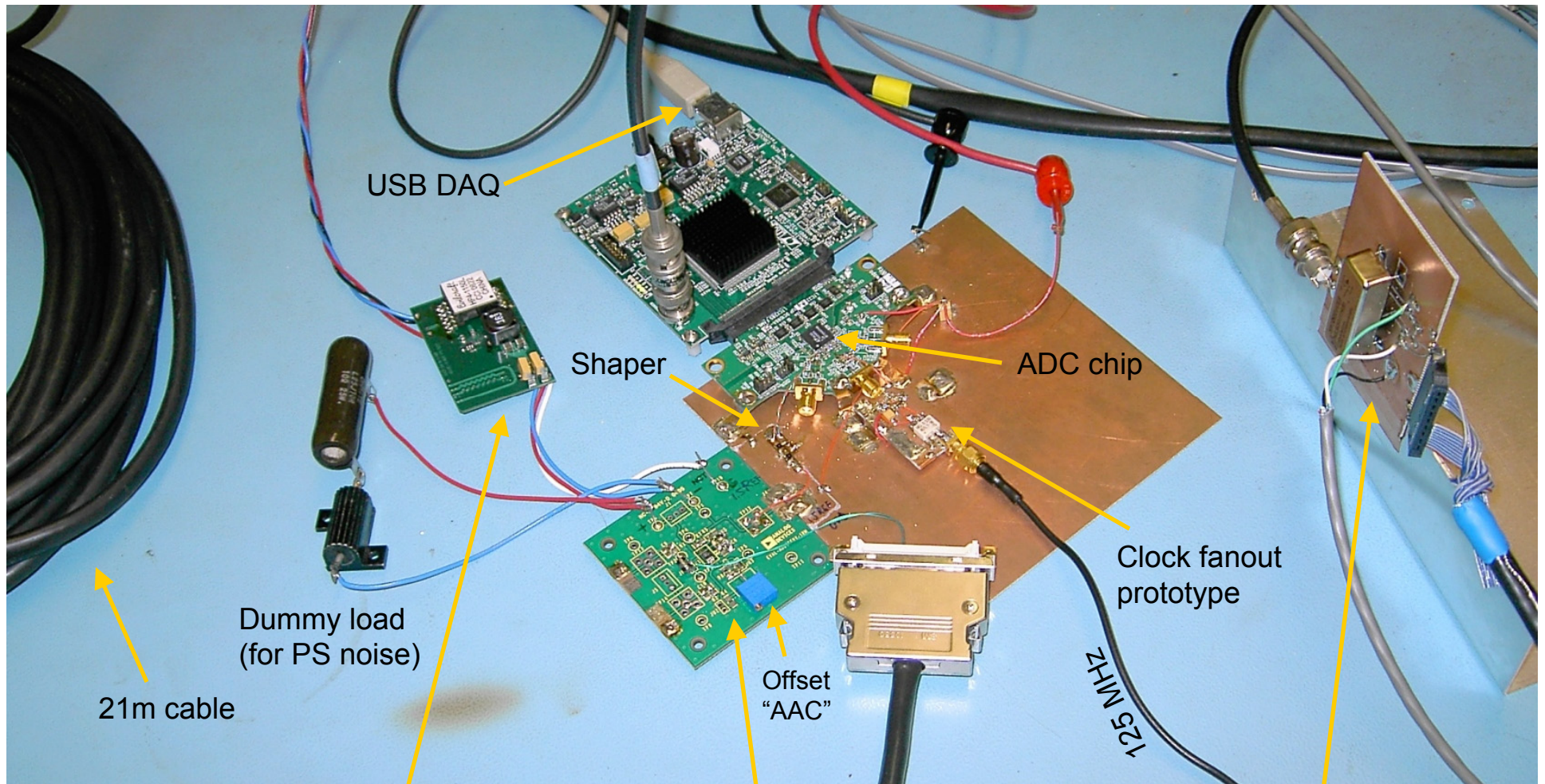
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8/22/2008

The development prototype (single channel)

Presently has essentially the real implementation of line receiver, eq, shaper, ADC, clock fanout, PS for line receiver.
Missing: Offset DAC (not needed), ADC PS (should do), FPGA (not needed).



Switching PS
24V → isolated $\pm 5.5\text{V}$, 18W

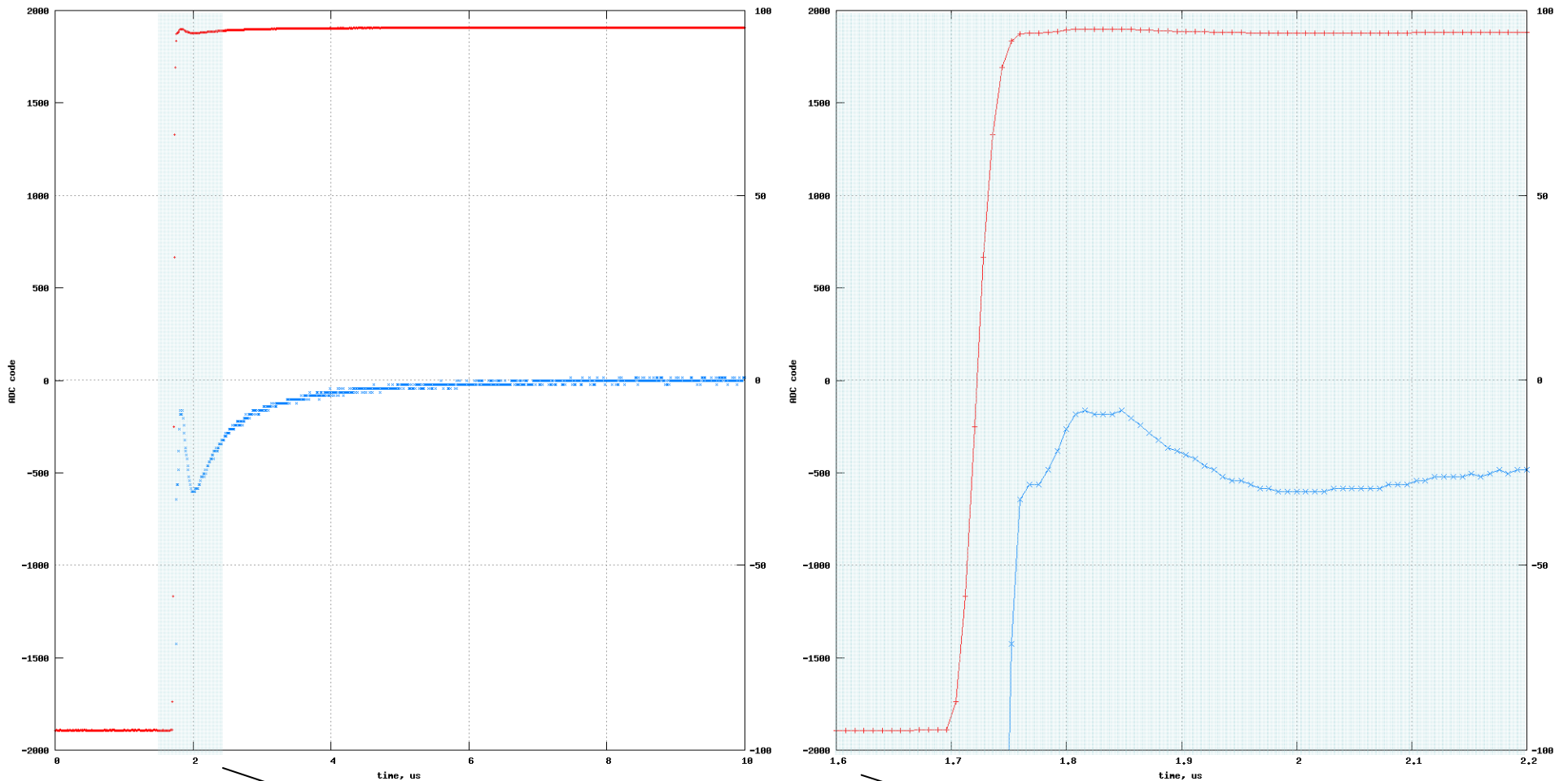
AD8129 line receiver
with equalization circuit

Precision pulse generator
(mercury reed relay)

Step response of cable – ADC system

OUR GOAL: Provide a faithful measurement of *the signal driven by the ASIC*, i.e., into terminated cable / ADC system

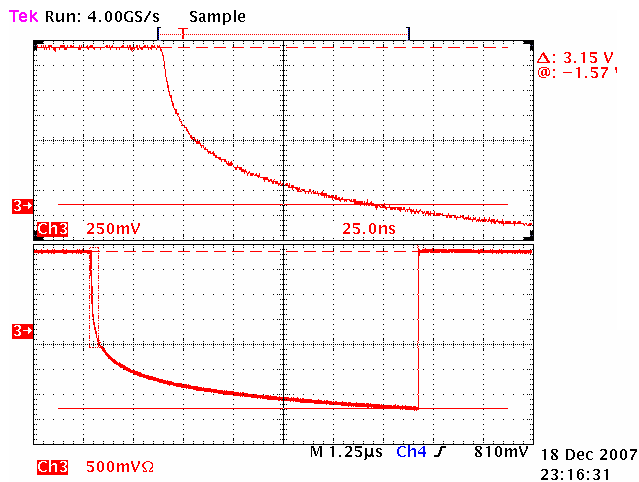
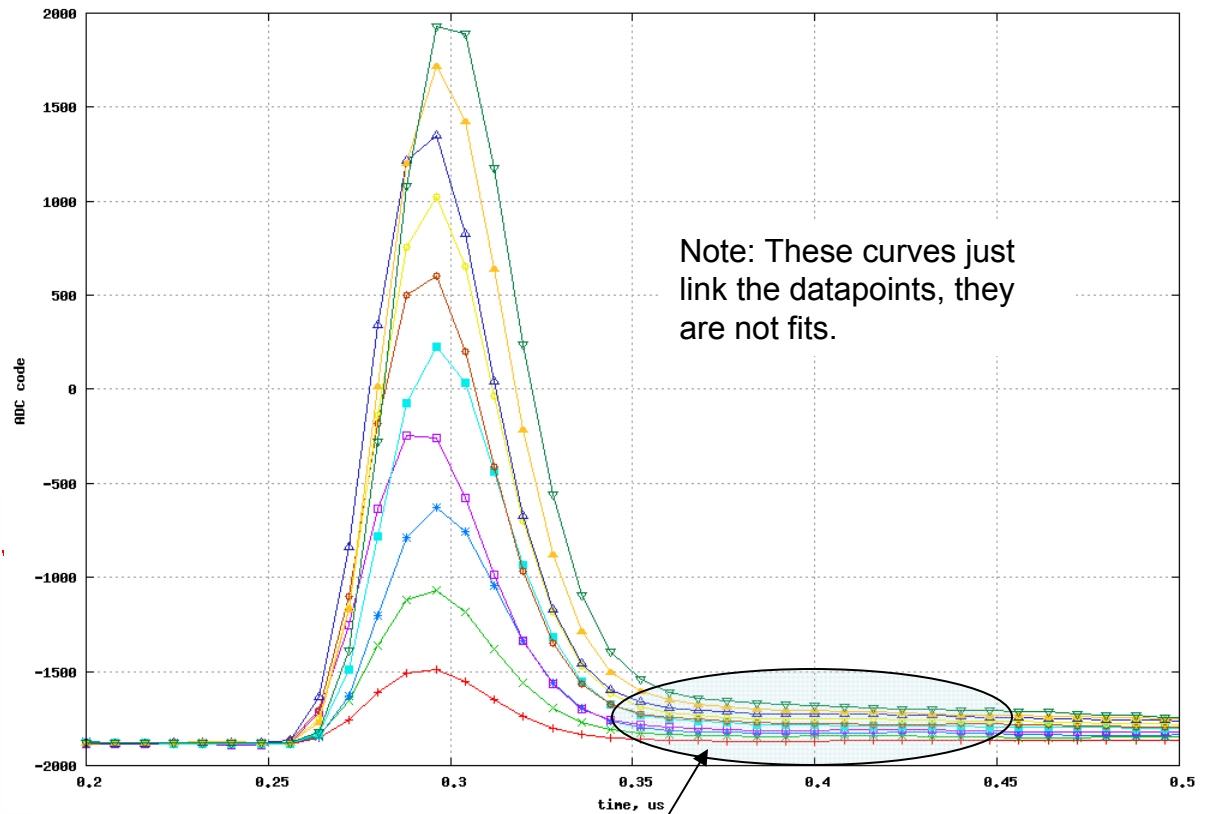
- Settles to <1% in 60 ns – if cable temperature is held within $\pm 5\text{ }^{\circ}\text{C}$
- Peaking time $\approx 28\text{ ns}$ for impulse input (about $\frac{1}{2}$ the step risetime shown here)



Detector-equivalent pulse response of ASIC – cable – ADC system

- Peaking time ≈ 30 ns
- Full width ≈ 90 ns at $1/_{10}$ max
- Overall gain to pulse height ≈ 8.9 ADC units / electron
- Gain is a little less than present receiver/shaper feeding 1 Volt Struck ADC

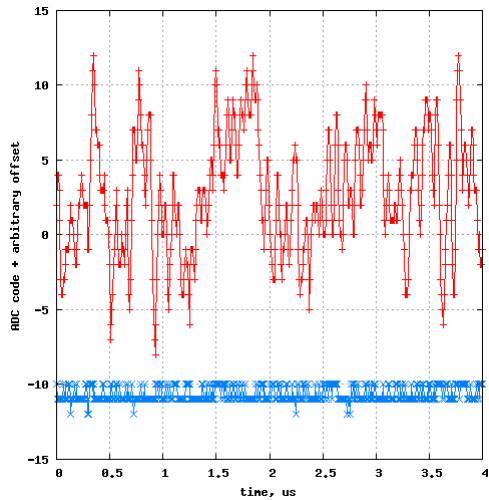
47 to 470 electrons, assuming 5×10^4 gain and $t_0 = 1.38$ ns



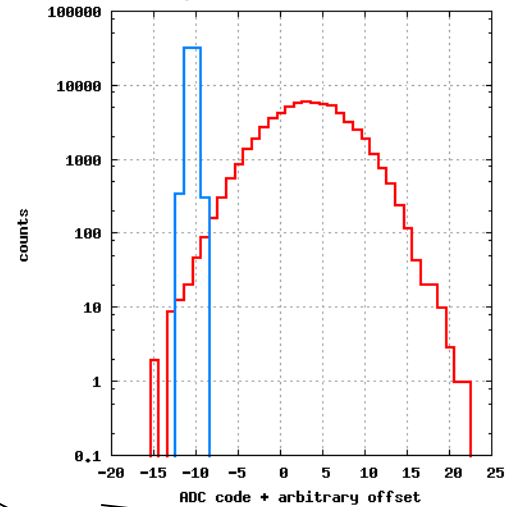
We could decide to adjust ADC equalization filter components (or use DSP) to better cancel the remaining tail. Decide it later, after some testing with detectors / GAS-2 / ADC. Remember, (PVC) cable temperature also affects the tail.

Noise

Time-domain noise, ASIC on/off

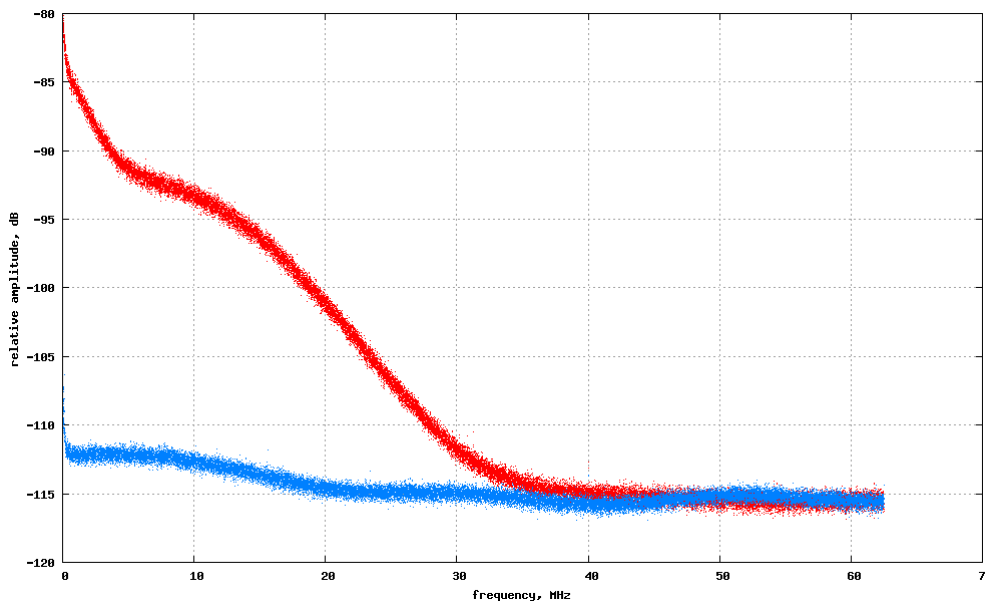


Noise histogram 64k consecutive samples, ASIC on/off



$\sigma = 4.24$
 $\sigma = 0.52$

Noise power spectrum, 64k Hann window FFT, ASIC on/off

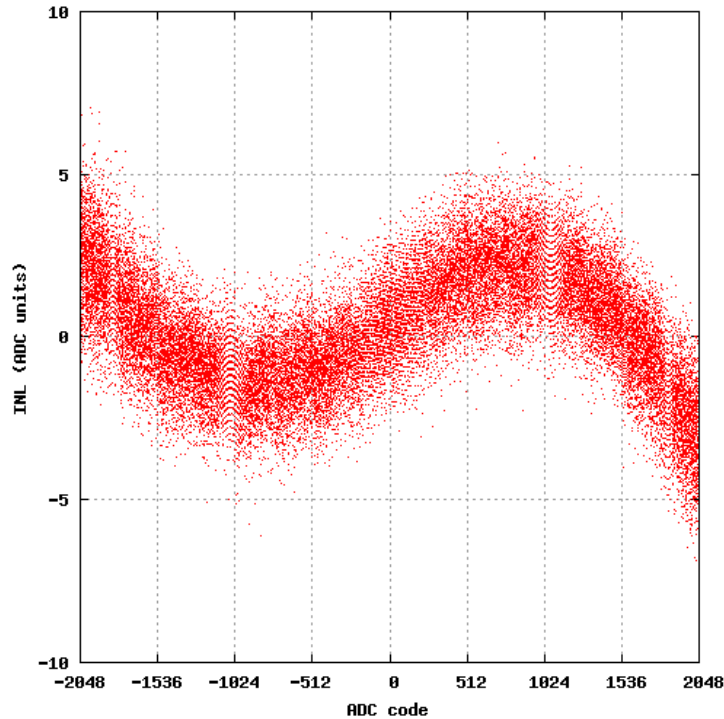


Conclusions

- Cable + ADC noise is negligible, even with gain set a little low as it is now
- Spectra look good, no spurious stuff such as PS ripple
- 12 bits is plenty! I don't see any justification for 14 bits, performance is not limited by ADC binning
- At 2pF detector capacitance, the ASIC *in this system* delivers effectively a noise $\sigma \approx 23,800$ (total) electrons

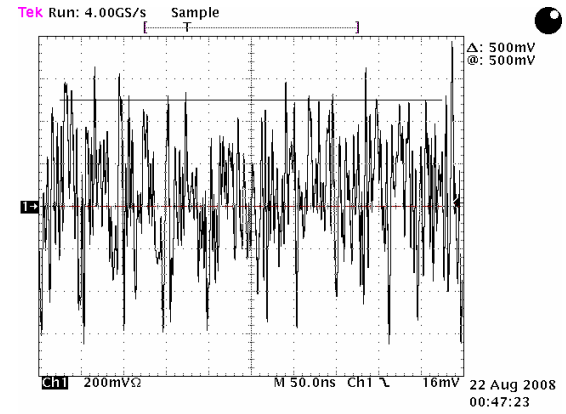
Linearity and Common-Mode Rejection

(Integral) linearity (from 500 kHz sine fit)

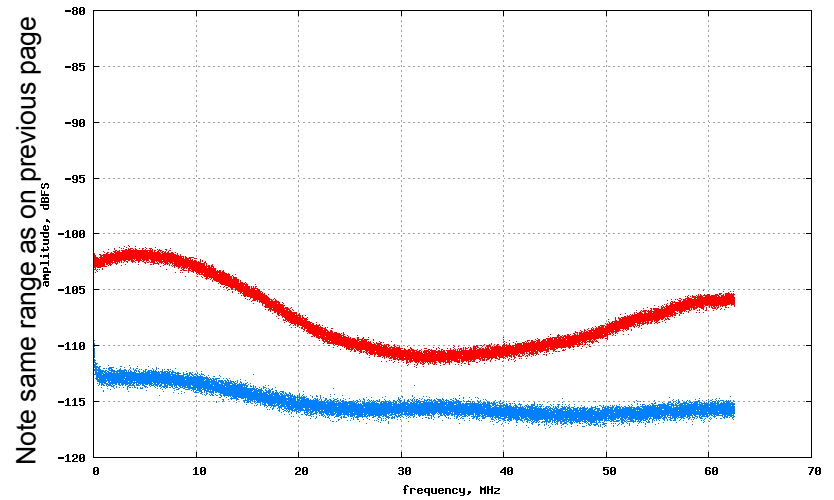


$\pm 0.12\%$, mainly limited by AD8129 characteristics

Inject a harsh common-mode noise signal:



Noise w/ and w/out the common-mode noise signal



That much common-mode noise contributes only about as much as the ASIC noise with no detector capacitance – good!

What will be the production test plan?

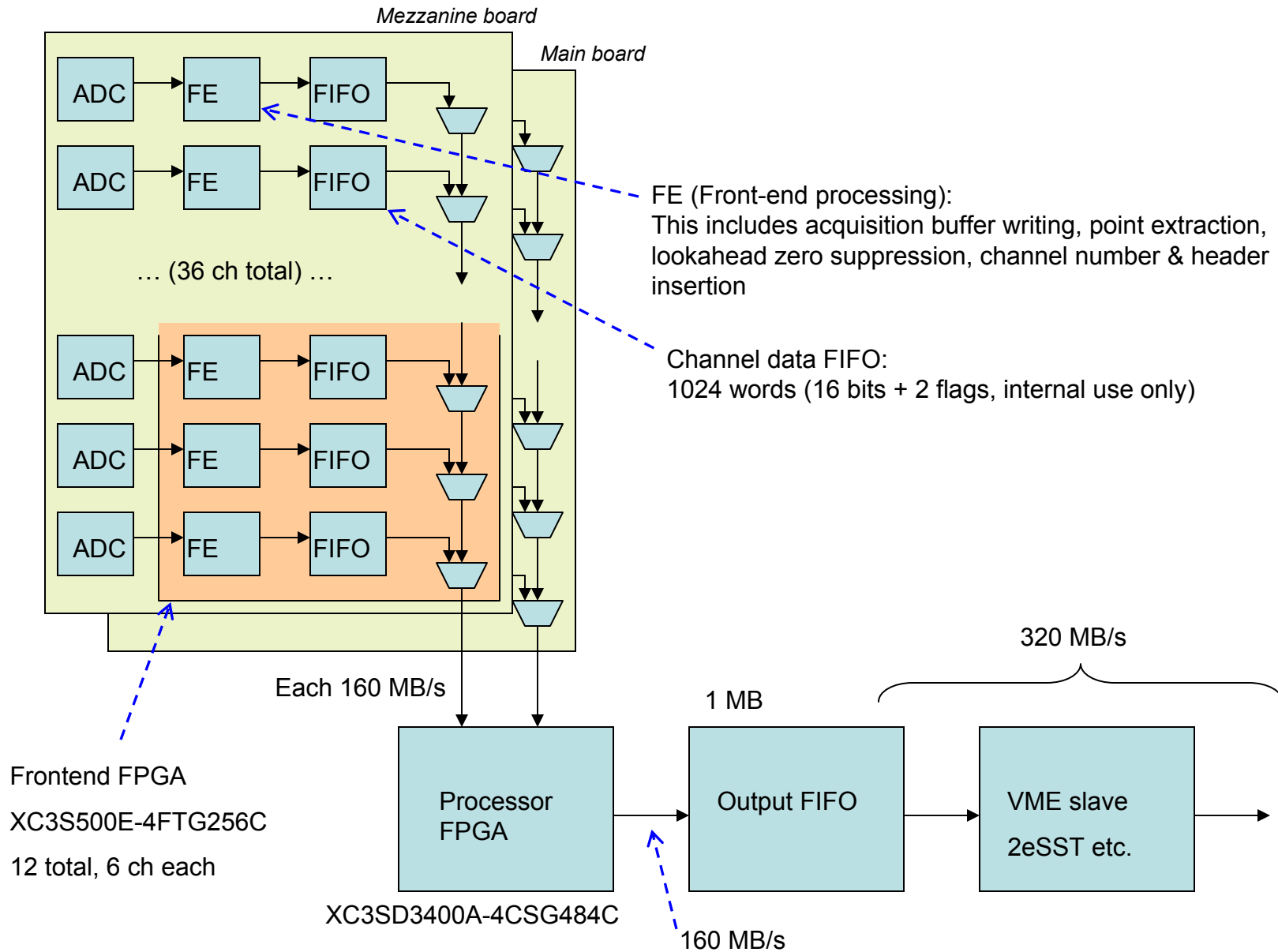
Some highlights:

- All supply voltages probed, input supply currents monitored (+5, +3.3, ± 12 from backplane)
- DC transfer function (including linearity and missing-codes check), each channel, offset DAC \rightarrow ADC
- Noise histogram, each channel
- Connect to input test fixture, standard pulse (step?) response check on each channel, synchronous to clock, i.e. tests also for clock problems.
- Data integrity checks from read/write test patterns and push test patterns to output FIFO

The above will be done at a semi-automated test station consisting of:

- VXS crate (JLab?) including CPU and trigger/clock source (VXS)
- Current monitor VME extender
- Perhaps an external computer to run the test software, at least something for operator interface
- Three plug-in test source modules, probably also involving a signal generator
- Benchtop DMM
- Other test equipment will of course be needed (and available) for diagnosis and repair...

Reminder / update on the ADC board datapath architecture



Status of the ADC125 design work

We were supposed to have a module by this time... Where is it?

- | | | |
|--|---|---|
| <input type="checkbox"/> Input connectors and routing | <input checked="" type="checkbox"/> Proc – FIFO routing | <input type="checkbox"/> Main – mezzanine copy/paste |
| <input checked="" type="checkbox"/> Line receiver / eq | <input type="checkbox"/> Proc FPGA pinout/symbol | <input checked="" type="checkbox"/> ADC, FPGA procurement |
| <input type="checkbox"/> Offset DAC | <input type="checkbox"/> FIFO – VME FPGA routing | <input type="checkbox"/> Misc. parts procurement |
| <input checked="" type="checkbox"/> Shaper | <input type="checkbox"/> <u>VME FPGA – xcvr routing</u> | <input type="checkbox"/> Fabrication |
| <input checked="" type="checkbox"/> ADC | <input type="checkbox"/> VME FPGA pinout/symbol | <input checked="" type="checkbox"/> FE FPGA frontend |
| <input checked="" type="checkbox"/> ADC – FPGA routing | <input checked="" type="checkbox"/> P1/P2 routing | <input checked="" type="checkbox"/> FE FPGA backend / readout |
| <input checked="" type="checkbox"/> FE FPGA readout daisy-chain | <input type="checkbox"/> <u>+1.2V PS</u> | <input type="checkbox"/> Proc FPGA datapath |
| <input checked="" type="checkbox"/> FE FPGA pinout/symbol | <input type="checkbox"/> <u>+2.5V PS</u> | <input type="checkbox"/> Proc FPGA trigger handling |
| <input checked="" type="checkbox"/> Line receiver PS | <input type="checkbox"/> Config flash | <input type="checkbox"/> VME FPGA datapath |
| <input type="checkbox"/> <u>Virtual ground / CM ref</u> | <input type="checkbox"/> JTAG routing | <input type="checkbox"/> VME FPGA controls |
| <input type="checkbox"/> <u>ADC analog PS</u> | <input checked="" type="checkbox"/> Local clock distribution | <input checked="" type="checkbox"/> VME FPGA configuration |
| <input checked="" type="checkbox"/> Line receiver PS prototype | <input checked="" type="checkbox"/> Full signal path prototype | <input type="checkbox"/> Programmer's reference manual |
| <input type="checkbox"/> <u>ADC analog PS prototype</u> | <input type="checkbox"/> Thermal analysis | <input type="checkbox"/> Testing & evaluation |
| <input checked="" type="checkbox"/> Sample clock tree | <input checked="" type="checkbox"/> Mezzanine stacking conn. | <input type="checkbox"/> ADC125 design report |
| <input checked="" type="checkbox"/> Clock / trig inputs P2 + VXS | <input checked="" type="checkbox"/> Board materials & layer stack | <input type="checkbox"/> Delivery for FDC/CDC work |
| <input checked="" type="checkbox"/> Clock / trig receiver | <input type="checkbox"/> Power plane segmentation | |
| <input type="checkbox"/> Pulser (to detector) | <input type="checkbox"/> Silkscreen scrub | |
| <input type="checkbox"/> FE – Proc routing | <input type="checkbox"/> Final channel copy/paste | |

Green is done.

Blue are "final steps" to fabrication.

Underlined are the tasks I'm currently working on.

The mainboard layout today

Please note, it looks “empty” but there is a lot of trivial copy/past that will happen!

The screenshot displays the P-CAD 2006 PCB software interface for a project named 'gluex_adc.pcb'. The main workspace shows a detailed PCB layout with a central vertical channel, various components, and a dense network of traces. The interface includes a menu bar (File, Edit, View, Place, Route, Options, Library, Utils, Tools, DocTool, Macro, Window, Help), a toolbar with various icons, and a status bar at the bottom. The status bar shows settings such as '1.5000', '182.0000', 'Abs', '0.5000', 'M', 'Bottom', '0.1800mm', and '(None)'. A vertical text annotation on the left side of the workspace reads 'DON'T FORGET THE HANDLE/PANEL HOLES!!!'. A text box on the right side of the workspace contains the following information:

P0 CONNECTOR PLACEMENT
HOWEVER IN THAT DESIGN
PLACEMENT NEEDS TO BE

PLANE USAGE:
(THE "DEFAULT" NET IS LISTED FIRST)

GND1: ground
PWR1(L3, lowest impedance): +3.0A, +2.5D,
and: +5VME, +5FUSED

GND2: ground,
and: +5VME

PWR2(L7): +1.2D, -VRX
and: +5VME, +5FUSED

GND3: ground, VIP5
PWR3(L9): +1.2D, +VRX, +3.0A(for clk/trg in),
and: +12VME, -12VME, +3.3VME, -12VME

CAUTION!!! BE CAREFUL IN PREPARING GERBER AS I USUALLY DO.

need to consider (ask Sierra):
FR406, FR408, or GETEK material???

what is the cost implication?
what is the reliability implication?
I need to calculate the loss factor effect (

channel pitch 8.2mm (leaves 233.35 - 2x2.5 - 36x6.2 = 5.15 mm "extra")

Click <Left> to single Select, <Ctrl><Left> for multiple, or drag for block select.

Contract status

It started about 10/7/2007 (according to my IUCF effort reporting)

As of this week:

- Labor 520 hours – 51% of budget (1015 hours)
- Materials \$10,094 (including \$6,791 for ADC chips) – 39 % of budget

Performance: Average (over whole period) time committed \approx 32% – is 64% of planned

Recently, 104 / 185 hours

I can offer excuses from other projects, of course, but that is not all so helpful...

Billing status:

- Should have billed some time ago, but...
- IU accountants mistakenly applied overhead although it was supposed to be waived for this project as a capital construction effort...
- Then they realized it and have taken an inappropriately long time to fix it...
- Because of all that, they haven't yet sent a bill...
- I am told that one will be sent by about 9/8