

Nuclear Physics Division

*Fast Electronics Group &*

*Data Acquisition Group*

# Description and Requirements for the VME

# Trigger Interface and Distribution (TID) Module

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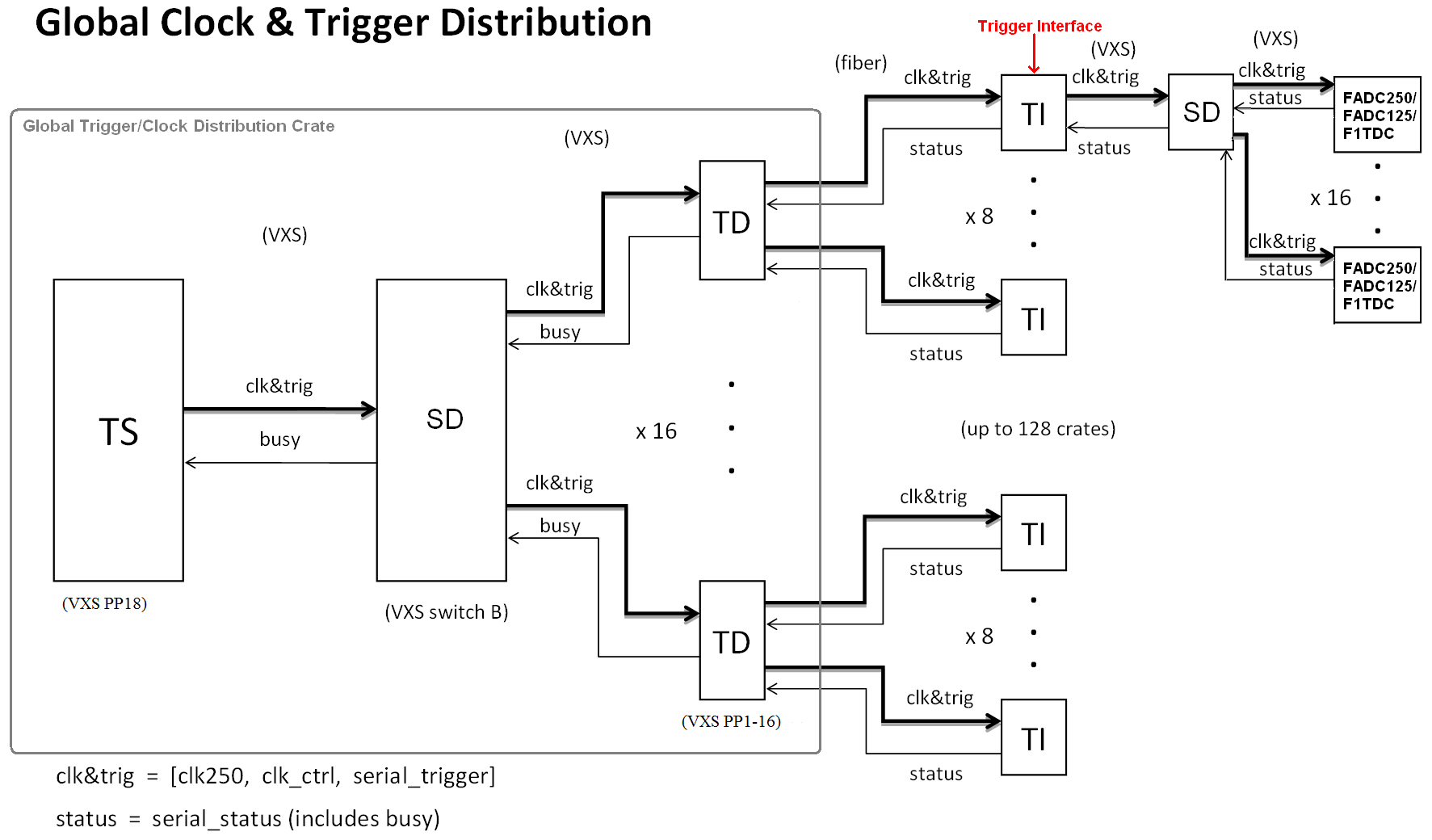
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# 1 Introduction

The Trigger Interface and Distribution (TID) module is being designed for the Jefferson Lab 12GeV upgrade, mainly for Hall-D[ (Collaboration, 2009)] and Hall-B[ (Collaboration C. , 2009)], with other experimental Halls [ (experiments, 1990)] compatibility. This module is responsible for distributing Trigger signals and interfacing with Front-end readout crates to provide a low-jitter system clock and fixed latency trigger signals in the data acquisition crates. The modules also merge the front-end data acquisition crate status and generate a BUSY signal to request to pause the trigger. Figure 1a shows the placement of the TID modules in the global trigger distribution scheme in Hall-D setup.

**Figure 1a:**



Depending on the PCB stuffing and mode settings, this module can sit in the Global Trigger/Clock Distribution Crate [ (Chris, 2009)] to fan out trigger and clock to the front-end crates, which is the functionality of Trigger Distribution (TD) [ (Raydo, 2008)] modules; or sit in the front-end data acquisition crate to send triggers to the Signal Distribution (SD) [ (Cuevas, 2008)] module and Crate Trigger Processor (CTP) [ (Chris, Gloabal Trigger Processor, 2009)], which is the functionality of the Trigger Interface (TI) [ (Ben, 2008)] module. The TID has simple Trigger Supervisor (TS) [ (Ed, 2010)] functions built in. The TID can act as a subsystem trigger supervisor when used independently. With other TIDs, a subsystem with up to eight crates can be setup without real TS module. The TID also has the flexibility to select the trigger and clock inputs from central trigger system or local (sub-system) trigger system.

**2 Purpose of the module**

The TID in the global trigger distribution crate receives trigger/clock signals from the SD and fans out the signals for up to eight crates in the data acquisition system. The global trigger distribution crate is designed to house up to 16 TID modules, which provides trigger and clock for up to 128 crates. The TID distributes the following signals to each front end crates: global system clock, trigger words, and a custom serial link to establish a fixed latency from the trigger Supervisor to front end crates. In addition, the TID will receive status information from each crate that will be used to generate a ‘busy’ signal and also track various status registers of the front-end crates.

The TID in each front-end data acquisition crate connects to a TID module in the global trigger distribution crate. This is done using a full-duplex fiber link, which provides a 16bit word every 16ns. This link uses a reference clock derived from the 250MHz global pipeline clock allow a trigger word to be distributed every 4 global pipeline clock cycles. The TID receives trigger words from the TS and depending on the trigger word type the TID can issue a crate level trigger condition, which is signals using 3 trigger bits: Trig1, Trig2, and Sync through the VXS switch port B. The trigger bits are sent to a Signal Distribution (SD) module that distributes these signals to all front-end modules in the crate. The TID module also accepts status signals from the SD module, which is the logical OR of the status signals from all front-end modules. These status signals can be transmitted back to the TS through the fiber optic link to slow down or inhibit further distribution of triggers until the status has been resolved. The status includes a WARNING and a BUSY. When the WARNING is set, the front end boards are requesting for trigger rate slow down; when the BUSY is set, the front end boards are requesting for trigger inhibit. The assertion of a status signal will create a dead-time in the data acquisition system which should be a rare occurrence since the data acquisition is being designed to handle the full trigger rate that can occur from the physics events being captured. The dead time will be monitored and recorded by the Trigger Supervisor board.

The data from TID can also be sent to Signal Distribution board, in parallel with the TID to ROC VME data transfer, through a 250 Mbps (or 500 Mbps) serial link on the P0 backplane. This provides a redundant data readout path.

The TID module is implemented as a 6U VXS payload module with VME64x connectors. It is backward compatible with VME64 and backward compatible with Trigger Supervisor Rev2 module. The TID in Global trigger crate may have different front panel from the TID in the front-end data acquisition crate.

**3 Functional Description**

**3.1 General discription**

# Figure 3a shows the block diagram of the TID module, indicating the major components used in the design. The HFBR-7934 is the multi-channel (4 Rx, 4 Tx) fiber link that the TID fans out/receives a low-jitter (<2ps RMS) 250MHz global pipeline clock, serialized 16bit trigger words, and a fixed latency signal used in producing a fixed latency trigger. The AD9510 is the main clock driver and gets synchronized lower frequency clocks. The Xilinx XC5VLX30T is used to encode/decode the trigger words at 16ns, to interface with the VME, to control the working mode etc. The P0 is compatible with the VXS payload slots, which matches with GTP, CTP, SD positioned in switch slots.

**Figure 3a: Trigger Interface Block Diagram**

**TI_block.tif**

**3.1 Fiber links**

# The HFBR-7934 is the multi-channel (4 Rx, 4 Tx) fiber optic link for the TID. For the TID in the global trigger distribution crate, all the eight HFBR-7934 transceivers will be installed, so each can support up to eight front end data acquisition crates. For the TID in the front end crates and global trigger crate, two HFBR-7934 transceivers will be installed, to receive the trigger/clock from central trigger and subsystem trigger.

**3.2: Clock Distribution**

One of the TID’s major functions is the pipeline clock distribution. There are five possible sources for the 250MHz clock: ‘P0 connector from SD in trigger distribution crate’, ‘onboard oscillator’, ‘external clock input from twisted pair cable’, ‘optical fiber input from central trigger in front-end crate’ and ‘optical fiber input from subsystem trigger in front-end crate’. The clocks from optical fibers need be de-skewed to synchronize with other crates in the system (and subsystem). The skew on the fiber could be as high as several ns, unless we choose low skew fibers. The TI\_rev3 co-ax cable de-skew technique will be used. The five clock sources will be multiplexed. There will be only one 250MHz clock running on the TID.

The clock is fanned out by the MC100LVEP111 2:1:10 clock driver. When the TID is used in the global clock/trigger distribution crate, the clock from P0 is distributed directly to the optical fibers (eight HFBR-7934 modules). The extra output from the clock driver will drive the *AD9510 and generate the onboard clock. In all the other cases, the clock will go to the* AD9510 first, and drive all the outputs.

Three clocks (with frequencies of 250 MHz, 125 MHz, 31.25 MHz) are distributed to the P0 backplane. One On-Semiconductors’ NB4N840M is used to switch the clocks, so that, the SWA and SWB can get any two of the three frequencies independently. A buffer is added to switch the signal from CML to LVPECL, as needed in the VXS specification.

The clock is also distributed to the connectors via ECL on twisted pair cables and VME P2 user defined pins via LVPECL for VME ADC or TDC modules, which are NOT in the VXS crate. The CAEN V1290 will get a synchronized 41.67MHz clock instead of the nominal 40MHz onboard oscillator frequency, because there will be too much effort involved to generate a system wide synchronized 40MHz clock, and the V1290 can be calibrated to accept the 41.67 MHz clock.

An eight-bit on board switch will be used to select the clock sources except for the AD9510, which will be configured by the FPGA firmware.

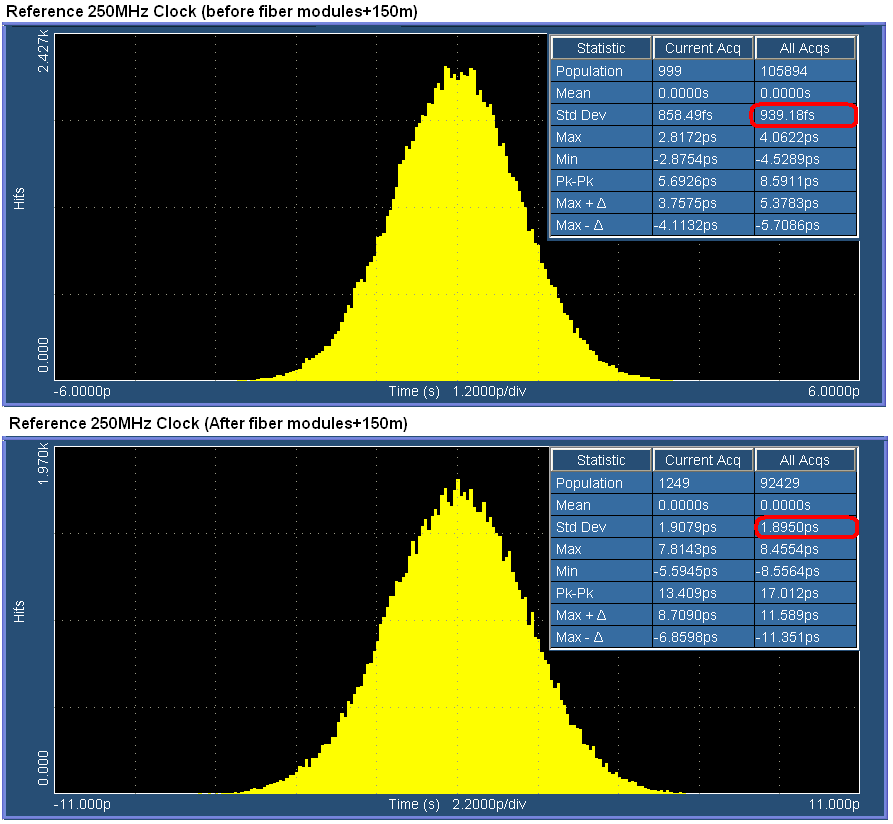
Firgure 3b shows the TID clock distribution diagram:

clock.tif

The clock is distributed in (LVP)ECL, or CML levels to keep the low jitter and low skew (faster propagation). The LVDS clock is used to drive the FPGA for easy termination.

The global 250MHz clock signal received over the fiber runs the L1 trigger pipeline electronics and nearly all of the front-end modules. Several front-end modules require this clock to have low-jitter and so the clock signal is buffered with components that contribute low-jitter, including the fiber driver and receiver. Figure 3c shows a measurement of the jitter contribution from the fiber driver/receiver pair, including a small increase in clock jitter (roughly 1.6ps additive jitter from the fiber driver/receiver with 150m of fiber between them) by Ben Raydo etal [ (Ben, 2008)]. Careful component selection, signaling, and layout techniques are employed to minimize overall clock jitter.

**Figure 3c: Global Clock (250 MHz) Jitter**



**3.3: Trigger Word**

A 1.25Gbps serial link operating over the fiber link, is used for distributing a 16bit trigger word to the TI every 16ns. There is also a link going in the opposite direction, allowing status words to be sent back to the trigger distribution crate. The 16bit trigger words are decoded as follows (TS->TID->TID flow):

Trigger strobe word – generated by the TS in response to the acceptance of a level 1 trigger. Upon receipt, the TI drives prompt trigger signals to the front-end modules. The TS transmits these with fixed latency relative to the accepted trigger. It is possible to add the timing information in the word to distinguish which quadrant of the 16 ns period the trigger is generated to be fully compatible with the 4ns pipeline design architecture. The trigger signal can be distributed in 4ns precision. This could potentially reduce the FADC readout window width, and reduce the event size.

Trigger content word – additional information about the trigger for use by the ROCs. It is queued in a FIFO and sent in any frame not used by a trigger strobe word. The TID matches the trigger strobe and trigger content words by the order of their reception.

Control Word – establish synchronization, request status, or other command. They can be queued in a FIFO and sent in any frame not used by a trigger strobe word.

Master Time Word – since the link must always be transmitting valid data to keep its latency fixed, bits [13:2] of the TS time is transmitted whenever no other word types are available. By continuously receiving bits [13:2] of the TS time, each TID can promptly detect if its subsystem has lost global synchronization (i.e. compare the global time with its own time). Otherwise, the loss of synchronization could only be detected at the event building stage. The continuous transmission of ‘known’ (i.e. predictable) data also allows one to monitor the integrity of the link.

Word type bit [13 12] [ 11 . . . . . . . . . . . . 0]

Time 0 0 lower 12 bits of TS time

Control 0 1 control or command

Trigger Strobe 1 0 trigger type/Trigger quadrant

Trigger Content 1 1 additional trigger data

(Bits [15,14] are used for error detection for all word types, this could be simply one parity bit and one TS busy bit)

The Trigger content word should include a trigger counter word, the TID can use this content word to check its synchronization if any trigger is missing by the TID.

The following defines the data format for the opposite direction of the link (TID->TID->TS flow):

Bit [15,14] Same as above, for parity check and crate busy.

Bit[15] Parity bit for word Bit[14:0]

Bit[14] represents the ‘busy’ status of the crate: ‘1’ = busy, ‘0’ = not busy

Bit[13] represents the “warning’ status of the crate: ‘1’=warning, ‘0’= not warning

Bit [12] indicates if a status word is available:

‘1’ = status word available, ‘0’ = status word not available

When the status word is available, Bits [11:0] represent the status word.

Figure 3d shows the diagram of the trigger word distribution:

trg_fan.tif

**3.4: Fixed Latency CLKSYNC**

The CLKSYNC signal is a 250Mbps serial line that operates very similarly to a standard UART operating in synchronous mode. This serial link allows a 4bit command to be sent at chosen 4ns points in time. CLKSYNC is synchronized to the master clock CLK250 and is sampled every 4ns cycle. The line is considered to be idle when more than 4 samples in a row are read ‘1’. A command is sent between idle times by sending first a ‘0’ followed by the 4bits that comprise the command, LSB first. After the command has been sent a final ‘1’ is sent so that the line will return back to the IDLE state. The encoding portion of this serial protocol is performed on the TS. Since the TID distributes this serial line over the fiber module, additional encoding (Manchester) is performed by the TID to balance the 1’s and 0’s of the line and to keep the maximum run length of the signal below the requirements of the fiber module. The TID decodes the CLKSYNC signal (Manchester and command). Careful design in minimizing CLKSYNC to the distributed master CLK250 skew guarantees a fixed latency link.

The CLKSYNC link is used in conjunction with a synchronous FIFO to enforce a fixed latency on the serial trigger link. On the TID module the parallel output of the trigger word is clocked into a FIFO using the FPGA built in Rocket GTP transceivers and the user clock, which is the same as the external 62.5MHz clock. Data words are clocked out of the FIFO using a 62.5MHz clock derived from (and in phase with) the system CLK250. At startup the FIFO is reset (0 words) and reading the FIFO is disabled. No words are written into the FIFO since the TS is not yet transmitting data words on the trigger link (i.e. received data valid signal is not asserted). Acceptance of triggers by the TS is also disabled. The TS starts transmission (time words) on the trigger link, and after a fixed number of 62.5MHz clock cycles issues a PREFILL command on the CLKSYNC line. In response to the PREFILL command, the TI enables continuous readout of the FIFO. There must always be a non-zero number of words in the FIFO to maintain a fixed latency link. This will be true if the number of words pre-filled into the FIFO x 16 ns is greater than the latency uncertainty of the link. In the case of the Rocket GTP, several words (e.g. 3 or 4) are enough when the latency is set to minimum as the elastic buffer is not necessary as all the clocks are the same or derived from the same 250MHz clock (no clock frequency difference). The TS must always be transmitting valid data to maintain the fixed latency of the link. This is illustrated in figure 3e:

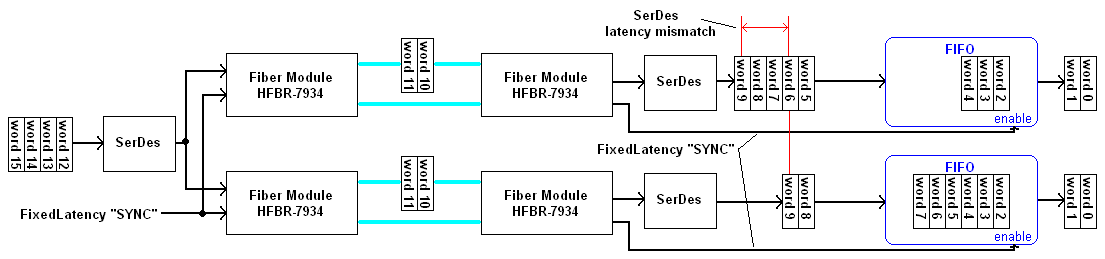
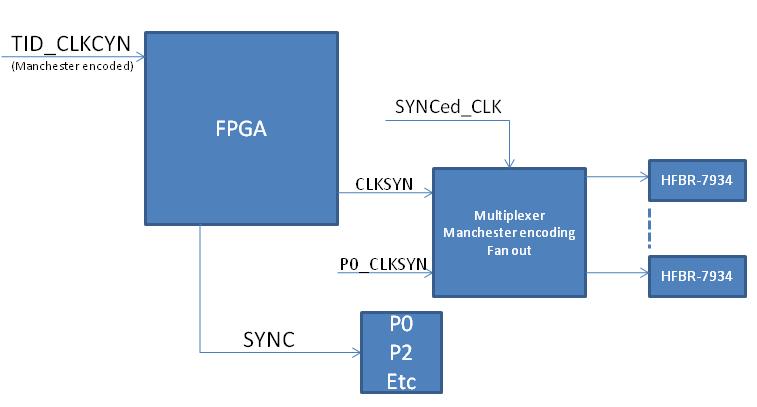


Figure 3e: Illustration of the Trigger synchronization process

The CLKSYNC link is also useful in ensuring that the lower frequency clocks derived in the TID from the distributed system clock (CLK250) have the same phase across all TID in the front-end data acquisition system. At startup, the TS issues a CLKSYNC command CLKRESET. This resets the clock distribution chip (AD9510) in each TI on the same CLK250 edge, assuring that the lower frequency clocks (125MHz, 62.5MHz, 31.25MHz) are in phase across the entire system. This command is sent before the TID sync command. The delay between them is determined by the maximum Rocket GTP reset recovery time, as the GTP clock is changed (AD9510 clock reset). The time is several ms.

Figure 3f shows the block diagram of the CLOCK\_SYNC distribution on the TID board:



**3.5: The Xilinx PROM programming.**

The Xilinx XCF32P PROM is used to program the FPGA. It can save two different versions of the FPGA (XC5VLX30T) firmware when used in master serial or master SelectMAP mode. It can save four different versions of the firmware when bit stream compression is used, in which case, only the slave serial and slave SelectMAP modes are supported. The PROM is programmed using VME with discrete logic decoding. It can be addressed in the VME64x crates by its geographical address. If it is in the crate without geographical address, only one TID in the crate should be addressed as geographical slot#0. To avoid conflict with other VME addressing, the user-defined address modifiers are used for the PROM loading. This approach is fully tested in CMS on LHC. One 25 MHz on-board oscillator is used to program the FPGA in slave mode, and used by the FPGA for slow control, for example, the VME to AD9510 serial control engine.

**3.6: Status passing**

The TID can merge the status together and pass on to upper level. Specifically, the TID can merge the status from the CTP and SD via P0 backplane and pass on to TID in the global trigger/clock distribution crate via optical links. The TID can merge the status from up to eight crates and send to SD (to TS) via P0 backplanes. Right now, only the BUSY is defined as status. We have the capability to add a less severe state, WARNING, to the status.

**3.7: Serial data to SD**

The TID can send data to the SD via a 250Mbps link, (it is possible to increase it to 500 Mbps using DDR techniques). This is implemented using the Xilinx SelectIO standard differential IO pin pair. In this case, the SD can be implemented as a data concentrator card to collect data from the VXS crate (the payload modules include FADC, FTDC, TID, etc). The TID will send data to SD on every trigger (event). This is another data readout path in addition to the standard VME readout. The maximum data rate is 50 MB/sec per slot. The full crate can reach up to 900 MB/sec assuming all 18 payload slots are used. This is the pilot implementation of hardware data acquisition system based on CMS/LHC experiences.

**3.8: Other functions (legacy compatibility)**

On-board connectors are used to interface with the TS rev2 module directly for backward compatibility, which may still be used in the experiment halls.

The TID has a general IO connector, which can accept up to eight different triggers, and it can also accept external clocks. Using these, some of the Trigger Supervisor functions can be implemented in the TID. The TID can serve as a subsystem trigger supervisor board with up to eight crates fan out capability. This will facilitate the (sub)system commissioning and subsystem test setups.

**4. Specification Sheet**

MECHANICAL

* Single width VITA 41 Payload Module. It will be position in the PP01 to PP16 in global clock/trigger distribution crate, or PP18 in front-end data acquisition crate and global trigger crate. It can also be plugged into any slots in standard VME crates without VXS.

HIGH SPEED SERIAL P0 and P2 INPUTS:

* BUSY LVDS signals
* I2C to VXS Switch A & B
* Clock, trigger and sync signals from SD when in trigger distribution crate.

HIGH SPEED SERIAL P0 and P2 OUTPUTS:

* Any two of these clocks (250MHz LVPECL Clock <3ps RMS Jitter, 125MHz LVPECL Clock <3ps RMS Jitter, and 31.25MHz LVPECL Clock <10ps RMS Jitter) to Switch slot#A and Switch slot#B.
* Trig 1 LVPECL Trigger Signal
* Trig 2 LVPECL Trigger Signal
* Sync LVPECL Trigger Signal
* 250/500 Mbps data (LVDS) to SD at per event basis

FRONT PANEL INPUTS & OUTPUTS:

* 250MHz LVPECL Clock Input & Output
* Trig 1 LVPECL Trigger Input & Output
* Trig 2 LVPECL Trigger Input & Output
* Sync LVPECL Trigger Input & Output
* Warning/Busy LVCMOS Input & Output
* Multi-Fiber Optic transceiver
  + HFBR-7934
  + POP4 compliant 4 channel Rx/Tx fiber module
  + Up to 150meter fiber link (with 500Mhz-km fiber)
  + Up to 300meter fiber link (with 2000Mhz-km fiber)
* CLK250 & CLKSYNC Outputs for Scope Alignment
* Totally up to eight HFBR-7934 for TID in distribution crate, and two HFBR-7934 in front-end data acquisition crate.

FIBER CHANNEL SIGNALS:

* CLKSYNC Fixed Latency Link
  + 250Mbps Serial Communication
  + Manchester Encoded
  + CLKSYNC to CLK skew variation < 700ps
* TRIGLINKTX/TRIGLINKRX
  + 1.25Gbps Trigger Word Line
  + Provides 16bit parallel data every 16ns
* CLK
  + 250MHz Clock <2ps RMS Jitter

INDICATORS: Front Panel:

* Power OK – Green LED; VME DTACK – Red LED

On board:

* Link Status – Green LED; FPGA programmed-Red LED

PROGRAMMING:

* VME to JTAG emergency loading with redundant On board JTAG connector

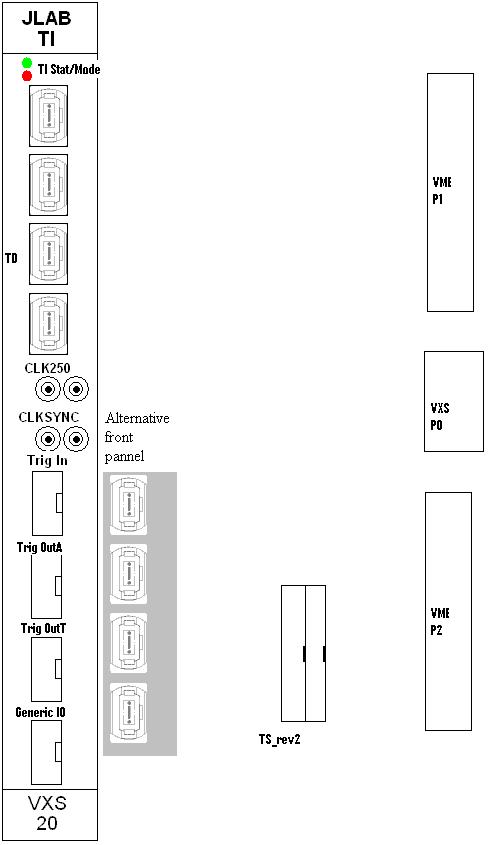
POWER REQUIREMENTS:

* +5v @ 5 Amps; -12V @ 1 Amp (From Backplane)
* Optional DC-DC converters for +3.3V, and Local regulators for other required voltages: +1.0V, +1.2V, +1.8V, +2.5V, +3.3V, and -5.2V.

ENVIRONMENT:

* Forced air cooling: Weiner standard
* Commercial grade components ( 0-75 Celsius)

Figure 4a shows the front panel and onboard connectors:



5 Programming Requirements (to be ignored right now. This part will be updated after firmware development)

4.1 Command, Status and Configuration Registers

VME to JTAG emergency loading:

The AM[5:0] user defined codes are used for this discrete logic. It is almost the same as A24 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E.

* Register: VME write

Configuration Registers:

Configuration Registers:

• **Address:** PORT\_ENABLE

**Description:** Enables Fiber Port and resets RX statistics. When

enabled, a busy status bit will be OR’ed with other enabled

ports and the final OR value will be supplied as a BUSY

signal to the TS over P0. Any status word received while a

port is enabled will be buffered in a FIFO waiting to be read

out over VME.

**Address Offset:** 0x0000

**Bit Description**

0 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 1

1 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 2

2 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 3

3 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 4

4 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 5

5 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 6

6 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 7

7 (r/w) ‘1’ enables, ‘0’ disables Fiber Port 8

8 (ro) ‘1’ = link up, ‘0’ = link down

9 (ro) ‘1’ = link up, ‘0’ = link down

10 (ro) ‘1’ = link up, ‘0’ = link down

11 (ro) ‘1’ = link up, ‘0’ = link down

12 (ro) ‘1’ = link up, ‘0’ = link down

13 (ro) ‘1’ = link up, ‘0’ = link down

14 (ro) ‘1’ = link up, ‘0’ = link down

15 (ro) ‘1’ = link up, ‘0’ = link down

31:16 X

• Address: RX\_STATUS\_BUFLENGTH

* Register: TRIGGER\_PULSE\_LENGTH

Description: The value in this register determine the trigger pulse width sent to the front-end module (through the SD module) in 4ns increments (0 = 4ns pulse, 1 = 8ns pulse, etc.). Either 4ns or 16ns makes more sense than the other settings.

Address Offset: 0x0000

Bit Description

3:0 (r/w) TRIG1 Min Pulse Length

7:4 X

11:8 (r/w) TRIG2 Min Pulse Length

31:12 X

* Register: TIME

Description: Returns bits [47:16] of the 48bit Time, which begins count after the RELEASE\_SYNC\_RESET command. The ticks are 4ns.

Address Offset: 0x0004

Bit Description

31:0 (ro) Time [47:16]

* Register : CLKSYNC\_ERRORS

Description: Detected bit error count of the CLKSYNC signal incoming from the TD module.

Address Offset: 0x0008

Bit Description

31:0 (ro) Error count

* Register: TRIGGERLINK\_ERRORS

Description: Detected word error count of the trigger word link incoming from the TD module.

Address Offset: 0x000C

Bit Description

31:0 (ro) Error count

* Register : I2C\_TRANSACTION\_ADDR

Description: This address species the starting address for an I2C read/write transaction.

* Register : I2C\_TRANSACTION\_WRITE

Description: This register initiates a read transaction starting at the address specified in the I2C\_TRANSACTION\_ADDR.

Address Offset: 0x0018

Bit Description

7:0 (wo) Number of bytes to write.

15:8 (ro) Indicates the number of acknowledged bytes for last I2C write transaction

30:16 X

31 set to ‘1’ to generate VME interrupt upon completion

* Register : I2C\_READ\_BUFFER

Description: This buffer contains the response data from an I2C read transaction.

1. Backplane pin out tables:

VXS P0 Pinout Table

|  |  |  |  |
| --- | --- | --- | --- |
| Payload slot#20 | | | |
| Pin name | Signal Description | Signal Level | Direction |
| DP1 | CLOCK\_C | LVPECL(DP) | PP18 🡪 SWA |
| DP2 | CLOCK\_D | LVPECL(DP) | PP18 🡪 SWA |
| DP3 | Not Used |  |  |
| DP4 | SYNC | LVPECL(DP) | PP18 🡪 SWA |
| DP5 | TRIG1 | LVPECL(DP) | PP18 🡪 SWA |
| DP6 | TRIG2 | LVPECL(DP) | PP18 🡪 SWA |
| DP7 | BUSY | LVDS(DP) | SWA 🡪 PP18 |
| DP8 | CTP/GTP\_LINK | LVDS | PP18 🡨🡪 SWA |
| SE1 | SCL | I2C (+3.3V) | PP18 🡨🡪 SWA |
| SE2 | SDA | I2C (+3.3V) | PP18 🡨🡪 SWA |
| DP23 | CLOCK\_A | LVPECL(DP) | PP18 🡪 SWB |
| DP24 | CLOCK\_B | LVPECL(DP) | PP18 🡪 SWB |
| DP25 | TOKEN\_OUT | LVDS(DP) | PP18 🡪 SWB |
| DP26 | SYNC | LVPECL(DP) | PP18 🡪 SWB |
| DP27 | TRIG1 | LVPECL(DP) | PP18 🡪 SWB |
| DP28 | TRIG2 | LVPECL(DP) | PP18 🡪 SWB |
| DP29 | STATUS | WARNING/BUSY | SWB 🡪 PP18 |
| DP30 | SD/GTP\_LINK  SD\_Data\_link | LVDS, 250Mbps | PP18 🡪 SWB |
| SE7 | SCL | I2C(+3.3V) | PP18 🡨🡪 SWB |
| SE8 | SDA | I2C(+3.3V) | PP18 🡨🡪 SWB |

Standard payload slots for TID in trigger distribution crate:

|  |  |  |  |
| --- | --- | --- | --- |
| DP23 | TRIG1 | LVDS | PP18 🡨 SWB |
| DP24 | CLKSYNC | LVPECL(DP) | PP18 🡨 SWB |
| DP25 | CLK250MHz | LVDS(DP) | PP18 🡨 SWB |
| DP26 | TRIG2 | LVPECL(DP) | PP18 🡨 SWB |
| DP27 | TOKEN\_IN | LVDS | PP18 🡨 SWB |
| DP28 | TOKEN\_OUT | LVDS | PP18 🡪 SWB |
| DP29 | SD\_Data\_link | LVDS | SWB 🡪 PP18 |
| DP30 | TRIG\_OUT | LVDS | PP18 🡪 SWB |
| SE7 | BUSY\_OUT | LVCMOS | PP18 🡪 SWB |
| SE8 | STATUS\_IN | LVCMOS | PP18 🡨 SWB |

1. VME P2 UserDefined pin table

Similar to this, but Row-C is used. The two adjacent pins are used as a pair for differential signals.

|  |  |  |
| --- | --- | --- |
| Pin name | Signal Name | Signal Level |
| C01 | SCL | I2C (+3.3V) |
| C02 | SDA | I2C (+3.3V) |
| C05 | CLK250\_P | LVPECL |
| C06 | CLK250\_N | LVPECL |
| C09 | CLK\_A\_P | LVPECL |
| C10 | CLK\_A\_N | LVPECL |
| C13 | CLK\_B\_P | LVPECL |
| C14 | CLK\_B\_N | LVPECL |
| C17 | TRIG1\_P | LVPECL |
| C18 | TRIG1\_N | LVPECL |
| C21 | TRIG2\_P | LVPECL |
| C22 | TRIG2\_N | LVPECL |
| C25 | SYNC\_P | LVPECL |
| C26 | SYNC\_N | LVPECL |
| C29 | STATUS\_WARNING | LVCMOS |
| C30 | STATUS\_BUSY | LVCMOS |

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