**FDC PCB Design Improvements**

FJB, 3/29/2010

**A. Sighting Fiducials**

1). Sighting fiducials on STBs and HVTBs: Cu vs. silk screen and tolerances on silkscreen. Need feedback from Keith on what he wants.

2). The sighting fiducials on HVTB are radially inward of solder pads. Is this an issue? The Cu elements will be floating. Also keep fiducials close to respective pads.

*It would be preferable to be silk screen (electrical) but definition and tolerances are not as good as copper. As these will serve for visual alignment, silk screen should be OK.*

*Need answer from Lubomir/Dan/Bill/Keith.*

**B. Glue Strips**

3). Finalize/confirm geometry between glue strip area and solder pads on STBs and HVTBs.

*Need answer from Lubomir/Dan/Bill/Keith.*

**C. Electroplating**

4). Verify plans for sense wire electroplating and length of sense wire solder pads in central region of STBs. How many many should be affected?

*The pads/vias we have now should be OK to accept connections from a custom test fixture with spring-loaded - to be designed. Need to keep vias free from epoxy.*

**D. Strain-Relief Holes**

5). Verify number and location of strain-relief holes on the HVTBs.

*Have 3-5 holes on each of the STBs and HVTBs, equally spaced and close to outer edge (~0.25”). These will be grounded, plated and direct-connected. Plastic wire ties will secure the various cables around the edge of the detector.*

**E. Pads/Routing**

6). Is it acceptable for vias on HV busses to be in line with solder pads. Will they be guaranteed flush with the pads so that wires cannot catch or snag on them?

*All exposed copper will be ENIG and should be level.Vias cannot be moved.*

7). Should the via on F49 be moved to slightly to the left?

*That won’t work. The bottom trace on –HV\_BUS\_1 (1004 PCB) to F49 is on the milling area. This was on the TOP on the previous version of the PCB and the HV did not hold. Move trace S49-R49 to BOT and have trace F50-F49 on TOP.*

8). Consider 2 vias when routing busses from/to different layers.

9). Keep –HV\_BUS\_2 away from R29, +HV\_BUS\_2.

10). Keep –HV\_BUS\_1 from crossing +HV\_BUS\_1.

11). +HV\_BUS\_3 crosses –HV\_BUS\_3. Can this be avoided?

*Crosses cannot be avoided completely but are on oposite layers and we have not seen any problems with the present prototypes. Moving traces away from other traces/componenets, as much as possible, is good practice.*

12). Check pad/trace on R1.

13). Move curved traces away from HV capacitor pads (also on C49, C50).

14). Add exposed copper pads (no vias) next to 1M resistors on signal side leading to connectors.

*This will be used for testing resistor connectivity.*

15). Add exposed copper pad to VTH lines.

*This will be used for testing resistor connectivity.*

16). R53 was moved because of gas manifold but it interferes with wire alignment.

*Needs answer from Bill.*