

**12GeV Trigger Workshop**  
**Christopher Newport University, Newport News, VA**

**Wednesday 8 July, 2009**

**Workshop Notes and Summary**

**Session I: 0900 --> 10:45**

Welcome and Overview -Chris Cuevas

-- Goals for the workshop

1. Review and discuss present requirements for the trigger systems of Hall D and Hall B, Hall C and Hall A.
2. Clearly identify new requirements for trigger system modules that have not been designed. Review recent success of two crate trigger module test station.
3. List requirements for "Global" trigger system:

**Session notes:**

There were many questions during the presentation which was useful to explain the details of each of the trigger module functions, and descriptions of the module features and functions. The prototype flash ADC module was described in detail and there were several questions about the resources that are presently used on the module's front end FPGA to manage the data processing modes and meeting the 200 KHz trigger rate requirement.

A discussion about the plans to implement an algorithm to extract timing resolution for each channel to <500ps resolution was exchanged and the Hall D FCAL group at IU has developed an algorithm that delivers acceptable results. Hai has started the implementation and firmware development work and has several data sets from the FCAL group to use for testing his FPGA code. The new algorithm will have to perform at the 200 KHz trigger rate and the module will provide a pulse charge value and a time value for each channel that crosses threshold. Presently the flash board provides a time marker of 4ns for each channel and a pulse charge value. (Pulse mode)

We talked briefly about the next revision of the module and the goal to reduce the component costs, and include new requirements of 12bit ADC and of course maintain the existing functions. The timing algorithm feature is a very important development and progress will be reported by Hai in the coming months.

There were several questions about how a single crate or two crates could be used in experiments (Hall A & C ) or for Users that will not have a Global Trigger Crate and associated modules. This was a good opportunity for discussion and raised a few **\*requirement\*** points that need to be investigated. Briefly, the addition of front panel input/output signals for both the CTP and TI should provide Users the flexibility to run a single crate in a stand-alone mode. The flash modules in conjunction with the Crate\_Trigger\_Processor could still be used to create a custom trigger for the channels that are in the crate, and outputs from the CTP or TI could be used in a JLAB 'legacy' DAQ system.

For CLAS12 (Hall B), the upgrade plans include the use of FastBus systems so we will have to review the signal requirements for those legacy systems and provide the proper signaling for level 1 accept, fast clear, and busy common signals. CLAS12 will use the flash modules for the several detector systems, and have given preliminary requirements for not only energy sum, but cluster finding algorithms that will be used in their level 1 trigger decision.

## **Session II: 11:00 --> 12:45**

DAQ System - Session 'leaders' David Abbott, Ed Jastrzembski

### **Session notes:**

Ed Jastrzemski presented the details of the trigger supervisor and global trigger system features. The trigger supervisor module will reside in a VXS crate as a payload module and receive trigger inputs from the Global\_Trigger\_Processor and other external sources. Ed explained how the TS distributes the common signals to the Trigger\_Distribution modules via the VXS backplane. Each TD module supports up to eight front end crates through a fiber optic link.

Special trigger event types and an optional trigger content word were explained and there were a few questions on how this trigger word would be used in an experiment. The event types included block modes, and calibration modes, and the discussion continued on the topic of changing modes by using the two trigger bits that is distributed to every flash module. I listed this as a ***\*requirement\**** because the present flash design does not change modes via the trigger bits. Presently, the mode is changed through VME configuration. For example, setting up the flash for raw-data mode is configured through VME commands. With the new requirement, the flash module would change modes depending upon the trigger bit settings. One could set up the flash for raw data mode at startup, and then the TS could issue a "Scaler" readout mode through use of the two trigger bits. The flash board would respond to the trigger bits and change modes for that trigger event.

Another ***\*requirement\**** was established after Ed explained the methods to implement multiple trigger "sessions". A simple partitioning idea was explained with up to 4 concurrent partitions supported. Implementation of the trigger partitioning 'sessions' will require a significant level of development, but it sounded as if this can be accomplished before commissioning the new 12GeV experiments.

Dave Abbott presented details and results of testing with the new Intel based GE Fanuc 7865 ReadOut\_Controller (ROC) that is planned for use with the 12GeV readout electronics. His presentation also covered the performance results with a few operating systems, and I believe the conclusion was to use a Linux OS on the ROCs. Dave also described more details of the plans for CODA version 3 with explanation of the event management methods.

It is clear that the raw data readout mode from the flash boards will not work at the 200 KHz trigger rate (requirement) because the event size becomes too large. The flash board readout performance has exceeded the 200 KHz trigger rate requirement in the "pulse-charge" mode, and we will have to review the data rates expected for the 72-channel flash boards that will be used for Hall D's Forward Drift Chamber readout.

Dave added another ***\*requirement\**** for the final versions of the CTP and SD in that we will need to dedicate a VXS pair from each switch card to the TI. Presently the communication link between VME and the switch slots are through the Trigger Interface module over an I<sup>2</sup>C slow serial link. The I<sup>2</sup>C link should remain, but to transfer scaler event data or other data on an event by event basis will require a faster dedicated link. The GE Fanuc ROC also provides a full duplex (Ethernet) 'lane' so this lane should be accommodated as an input to the Crate\_Trigger\_Processor through VXS. Presently the CTP does not expect high speed serial data from PayloadPort 17, which is the VME bus arbitration slot.

### **Session III: 14:00 --> 15:45**

Global Trigger - Session 'leader' Alex Somov

#### **Session notes:**

Alex Somov's presentation reviewed the existing trigger requirements for the GlueX experiment and showed recent trigger simulation results. One topic of discussion was the usefulness of the original 'track counting' trigger logic that was to be implemented on the CTPs for the Tagging system and the Time-of-Flight system. From Alex's simulations it seems that the TOF track count hits will not be useful for additional electromagnetic background rejection.

Discussions about how to connect or partition detector signals to each flash board started when Alex started to answer the question about the new hardware being able to handle the trigger equations. The Barrel Calorimeter was used as an example, and cabling each end of a BCAL segment to a flash board makes sense, and the summing would have to occur over a finite 'window'. Presently the flash board produces a sum of all the input signals every 4ns. Signals from each end of the BCAL may be tens of nanoseconds apart and would need to be summed within a window. The CTP does not provide a sum over a window, but in principle this could be another feature. The SubSystem Processor at the global trigger level will have to adjust and align the trigger data streams from multiple crates for each detector system, and ultimately the Global Trigger Processor will provide 'Trigger Window' functions to accommodate the sum timing from each subsystem. Plenty of discussion followed on this topic, and I believe more studies on the timing of pulses within the BCAL segments are needed to come up with any specific requirements at this point. I will add a point that the final design of the flash board includes all sixteen inputs to one FPGA, so summing and trigger logic between 16 channels is possible.

Alex continued with the topic of commissioning 'tools' and explained the idea of loading test 'vectors' to the front end flash FPGAs and starting a run. These test vectors (hit patterns) would be based on results of simulations for each type of trigger equation. During the commissioning phase, each crate or subsystem of crates would be loaded with test patterns, and the flash board would sum this data and send this trigger data upstream to the global trigger processor. The trigger equations in the GTP will be programmed to trigger on the specific test vectors, so the subsystem 'efficiency' and other performance information could be collected for commissioning results and/or troubleshooting. This type of test plan would also be a good way to test the stability of the entire trigger system including the verification of the complex subsystem trigger algorithms.

I did not capture in my notes any new requirements, and I believe Alex concluded that he thinks the present hardware design proposals will be capable of handling the required trigger equations planned for GlueX.

## **Session IV:-16:00 --> 17:30**

On-line and run control – Session ‘leader’ Elliott Wolin

### **Session notes:**

Elliott’s presentation started with an overview slide of the Hall D level 1 trigger system, which showed the **\*requirement\*** for external signals that will be needed for calibration and managing ‘pulsers’ for various detector subsystems. The Trigger Supervisor will have a direct connection to the Global Trigger Processor, and will also be designed to accommodate these types of external signals.

There were many other questions related to issues with how to program and configure the new trigger modules, and it is clear that there are many software applications to develop to configure and operate these modules during experiments. The topic of Graphical User Interfaces (GUI) for building trigger equation logic was discussed and it is not clear what group would develop these trigger tools and utilities. The DAQ/CODA group will develop the libraries that will be used to configure, monitor, and readout the front end electronics, including the global trigger hardware.

The topics of handling multiple trigger sessions, testing and diagnostic tools were discussed again, and other issues were raised. For instance, we have decided to use a particular style of fiber connector that will not make it easy to debug signals in the Hall. It is a strong suggestion to consider test ports or other peripheral test board designs now to aide in the system testing during the installation period.

Another important topic that was discussed and I will include it in a **\*requirement\*** list, is the point about having counters or ‘scaler’ channels assigned on each board in the trigger system. All boards in the system use at least one FPGA to process signals, so adding counters (scalers) to common signals will be relatively easy. This way each board could report trigger count, counts of BUSY, count number of times over sum, count event blocks, etc. These scaler values would be read out periodically or on demand for diagnostics to determine dead-time or to troubleshoot what crate/board are causing problems. There was some discussion about how to handle controlling scaler (counting) with an external ‘gate’ signal but I do not have notes to present an answer.

### **Summary of new \*requirements\***

1. Use the two trigger signals, Trig1 and Trig2 to change the mode of the flash board readout. Presently the readout mode is selected when the User programs the module before starting a ‘run’. Presently the mode does not change during a ‘run’. Using the two Trigger bits, the trigger supervisor can issue a specific readout mode for a given trigger event type. (Change mode for scaler readout data for example)
2. Dedicate a VXS differential pair from the TI to CTP and from the TI to the SD. Keep the I<sup>2</sup>C link, but a differential pair will be needed to transfer data from the two switch cards at a higher rate than the I<sup>2</sup>C allows. (The dedicated pair is not required to be a gigabit serial link.)
3. Add input/output signaling capabilities to the CTP and TI front panels. The number and type of signaling levels were not defined, but I/O signals will be required and allow for a number of useful features.
4. Global Trigger -- Implement multiple trigger partitioning “sessions”. Ed and David A. outlined a simple idea for up to 4 concurrent trigger sessions using CODA3.
5. Global Trigger – The Trigger Supervisor will need to manage external signals for calibration systems. Presently the TS is specified to connect directly to the Global Trigger Processor and the additional input/output to pulsers or other hardware will need to be managed.