Hall D Active Collimator Electronics
Engineering Notes and Recommendations

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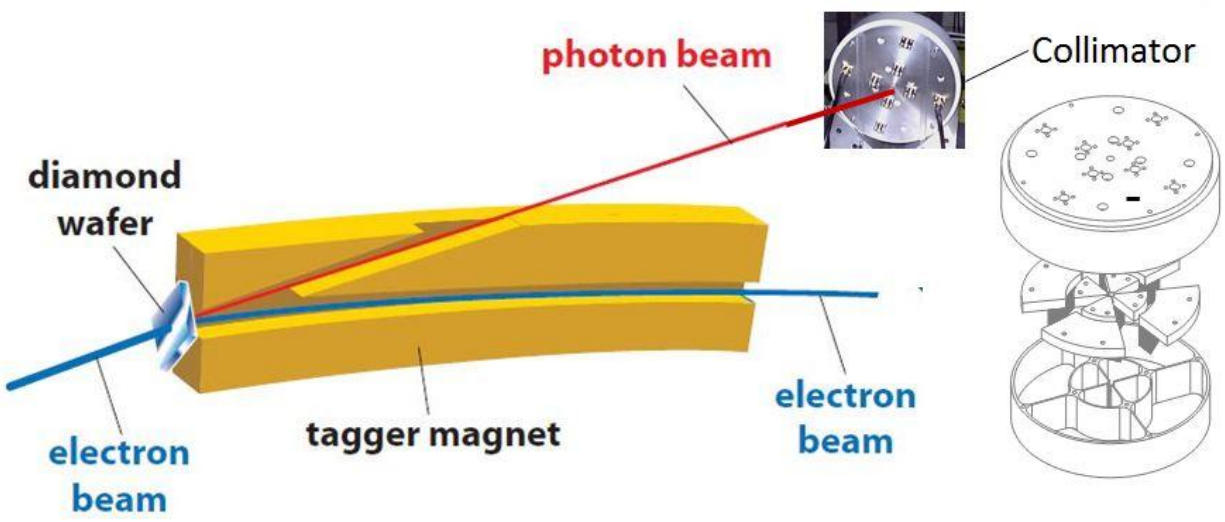
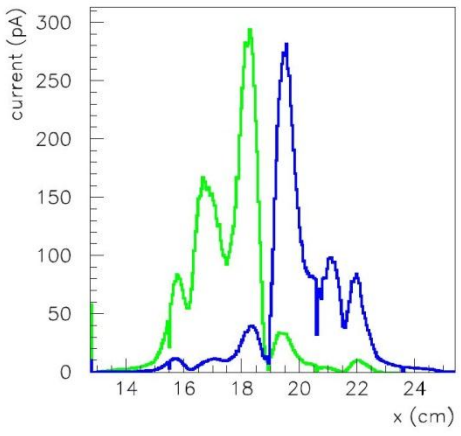
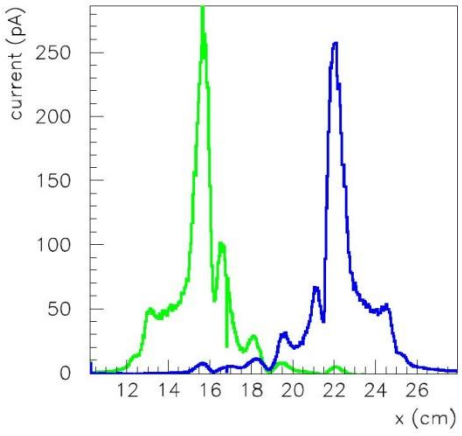
Background

The Hall D electron beam will pass through a diamond wafer radiator and then the tagger magnet will direct the electron beam to the dump. The photon beam continues straight ahead for approximately 80 meters to the Active Collimator in Hall D. An aperture in the center of the collimator will allow part of the photon beam to pass through and continue to the target while the intercepted photons interact with 8 tungsten plates with tungsten pins to generate current-based position signals.



The 8 collimator outputs are photon beam intensity and position dependent and divided into two sets of four; X+ Inner, X- Inner, Y+ Inner, Y- Inner, and X+ Outer, X- Outer, Y+ Outer, Y- Outer. The collimator is mounted on an X-axis stage that could be used for X position calibration. If the orientation of the collimator was rotated by 45 degrees then the X-axis stage could be used to calibrate both X and Y. The following plots show results from beam tests in Hall B from the X inner and outer +/- signal pairs.





Data acquisition electronics are needed to convert the collimator signals to positions for Ops and Physics and fast feedback electronics are needed to keep the photon beam steady at the collimator. The centroid of the photon beam at the collimator entrance must be measured within 200 µm RMS for electron beam currents from 500 pA to 5 µA and the position must be held to within +/-200 µm rms. Position measurements are to have a 1 kHz bandwidth for electron beam currents above 50 nA and beam current divided by 50 nA in kHz below 50 nA. Feedback control must have a bandwidth of 1 kHz and latency less than 150 µs. Development of a BPM and Active Collimator based fast feedback system is already included in the 12 GeV BPM account but the collimator electronics is not. The original Hall D fast feedback system requirements specified +/-10 V analog position outputs from Hall D provided collimator electronics.

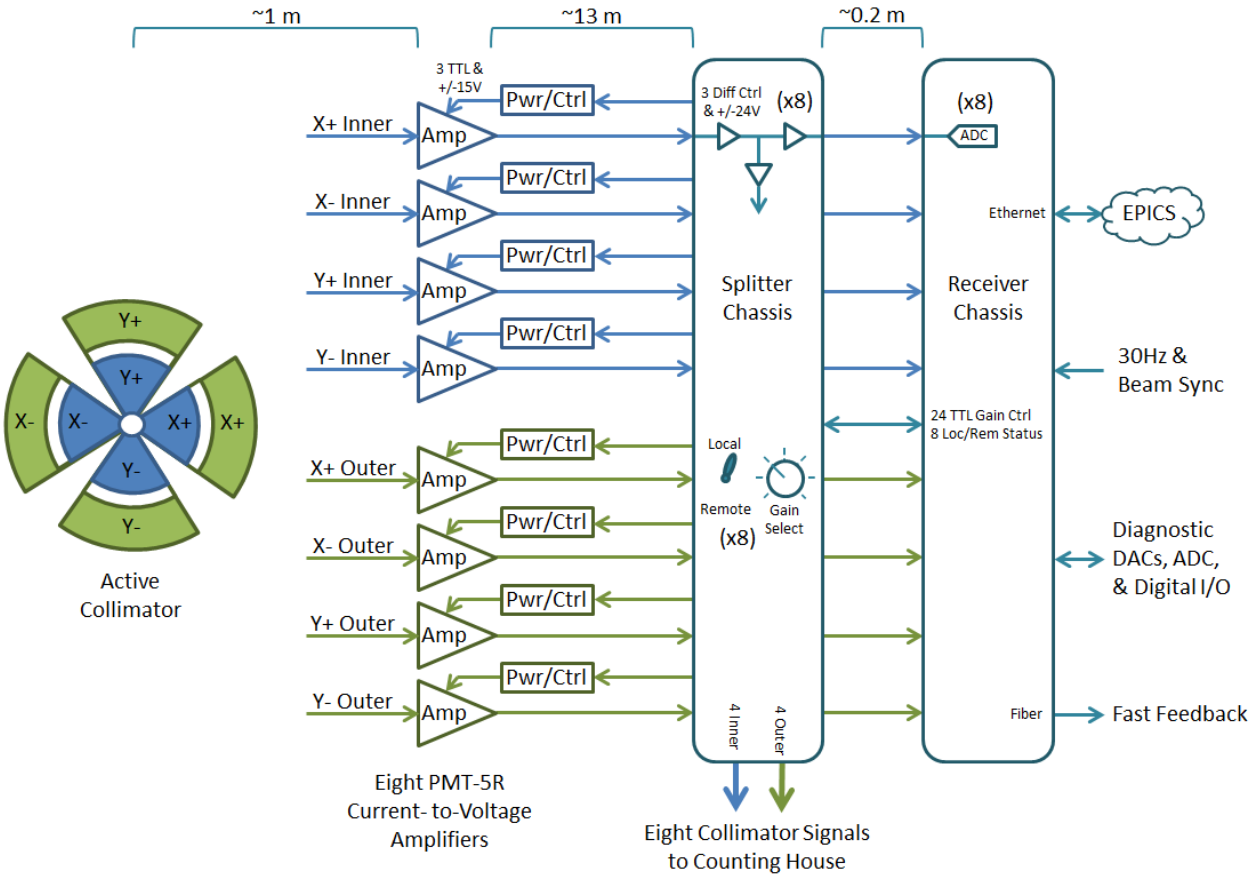
Existing Electronics

During testing in Hall B, the 8 collimator outputs were amplified with off-the-shelf current-to-voltage amplifiers (PMT-5R from Advanced Research Instruments Corporation, $950 each). The amplified signals were then sampled by a National Instruments PXI crate for post processing. The PXI crate will be replaced by custom JLab electronics and the Hall D data acquisition system. The same amplifiers will be utilized in the final design and it is assumed that these units and spares will be provided by Hall D. The amplifiers have TTL controllable gains from 10^{-6} to 10^{-12} A/V and a gain-bandwidth of 10^{13} Hz * V/A. They will be located within 1 meter of the collimator to preserve the signals and will require shielding. Amplifier specifications are below.

Input Impedance	1kΩ
Input Signal Range	1pA to 1µA per 1V output
Input Range Selector	Remote via 3 logic lines
Output Range	±10V
Output Impedance	100Ω
Power Requirements	±15V, 50mA
Physical Size	2.5 x 5 x 2 inches
Output Connector	BNC and 9 pin sub miniature D

Proposed New Electronics

The following diagram illustrates the layout of the proposed design solution. The Active Collimator outputs will be connected to the amplifiers, go through a Splitter Chassis and then get digitized by the Receiver Chassis. Each amplifier will have a Power & Control unit mounted with it that is fed by the Splitter Chassis. The Splitter Chassis will split the 8 collimator signals and provide local gain control of the amplifier gains. The Receiver Chassis will house an ADC/FPGA PCB and a PC104 input/output computer (IOC) for collecting data, calculating positions and running EPICS. 30Hz and beam sync will be used for synchronizing with the accelerator. Various diagnostic I/O will help with troubleshooting and allow for future expansion. A fiber output from the Receiver Chassis will provide the fast feedback system data for correcting the electron beam position.



Amplifier Power & Control

Format:	~3 x 2 x 1 inch box, custom PCB inside
Inputs:	3 Amplifier gain control pairs, differential, male 9-pin D (J1)
	+/-24 V & Ground, power, male 9-pin D (J1)
Outputs:	3 Amplifier gain control lines, TTL, female 9-pin D (J2)
	+/-15 V & Ground, regulated amplifier power, female 9-pin D (J2)

The PMT-5R amplifiers will be located within 1 meter of the collimator and will be shielded with lead bricks. They will be connected to the collimator with RG-58 cables with a SMA connector on the collimator end and a BNC connector on the amplifier end. A small Amplifier Power and Control unit will also be located with each amplifier to provide regulated +/-15 V and drive the TTL control signals. The amplifier outputs and the Amplifier Power and Control unit inputs will be cabled approximately 13 meters to a 19" rack in Hall D, away from radiation. The power/control cables will be shielded twisted-pair with 9-pin D connectors. The amplifier output cables will be RG-58 with BNC connectors on each end (the amplifier output impedance is 100 ohm but the signal is at DC so the cable impedance can be 50 ohm). It is assumed that the rack and 6U worth of space will be provided by Hall D (rack availability, location and cable lengths need to be verified). The amplified collimator signals and power/control cables will connect to the Collimator Splitter chassis in the rack.

Collimator Splitter

Format:	19” 2U Chassis, AC power, custom PCB inside
Inputs:	8 Amplified collimator signals, 0 to +10 V, single ended, BNCs
	8 Local/remote amplifier gain select toggle switches
	8 Seven-position amplifier gain select knobs
	24 Gain control bits, TTL, male 37-pin D (J1)
Outputs:	8 Buffered collimator signals to receiver, 0 to +10 V, single ended, BNC
	8 Buffered collimator signals to counting house, 0 to +10 V, single ended, BNC
	8 Local/remote gain select statuses, TTL, male 37-pin D (J1)

The Collimator Splitter chassis will supply +/-24 V power to the Amplifier Power and Control units as well as provide local control of the amplifier gain logic lines via eight 7-position selector knobs. The Collimator Splitter will also take in remote gain select TTL signals from the Collimator Receiver chassis. Local/remote gain switches will toggle between the select knobs and remote control and the switch statuses will be sent back to the Collimator Receiver for remote monitoring. These TTL signals will be connected using a male 37-pin D. The gain control signals between the Collimator Splitter and Amplifier Power and Control unit will be differential to ensure noise tolerance. The primary function of the Collimator Splitter is to take in the 8 amplified collimator signals and output two sets of the signals; one to the JLab Collimator Receiver electronics and another to the Hall D counting house for monitoring and/or data acquisition. The format of the buffered collimator outputs will be 0 to 10 V single ended (unless otherwise requested). The resulting collimator signals will be run to the Collimator Receiver and counting house using RG-58 with BNC terminations.

Collimator Receiver

Format:	19” 2U Chassis, AC power, custom PCB inside
	PC104 IOC running RTEMS and EPICS
Inputs:	8 Amplified collimator signals, 0 to +10 V, single ended, BNCs
	8 Local/remote gain switch statuses, TTL, female 37-pin D (J1)
	1 30 Hz, fiber
	1 Beam Sync, fiber
	4 Diagnostic DACs, +/-10 V, 18-bit, ≥100 kS/p single ended, BNCs
	1 Diagnostic ADC, +/-10 V, 16-bit, ≥100 kS/p, single ended, BNC
	~ 4 TTL, 2 Differential and 2 Fiber Spares
	1 IOC Ethernet, EPICS controls, RJ-45 (J2)
Outputs:	24 Gain control bits, TTL, female 37-pin D (J1)
	1 30 Hz repeater, fiber
	1 Fast Feedback, fiber
	~ 4 TTL, 2 Differential and 2 Fiber Spares
	1 IOC Ethernet, EPICS positions, RJ-45 (J2)

The Collimator Receiver will provide photon beam position data to EPICS, allow for remote EPICS control of the PMT-5R amplifier gains and send data to the fast feedback system. This will be achieved

with 8 ADC channels for sampling the collimator signals, TTL I/O for controlling amplifier gains, a FPGA for data collection/digital signal processing/controls, a SDRAM for local data storage, fiber inputs for accelerator synchronization, a fiber output to the fast feedback system, and a PC104 input/output computer (IOC) for computing positions/running EPICS. The Collimator Receiver will also have diagnostic and spare analog and digital I/O to aid in troubleshooting and allow for future expandability.

The 8 collimator inputs will come into the chassis through BNC connectors, be low-pass filtered with a 10 kHz cut off and then sampled by 16-bit ADCs at ≥100kS/s. The tentative plan is for the 8 channels of data to be digitally filtered by the FPGA and then stored in SDRAM until it is transferred to the PC104 IOC. The IOC will receive an interrupt when the data collection is complete, download the data, calculate and display the overall position and beam intensity, display waveforms of the positions/intensity and FFTs, determine if there was beam (on/off state), then rearm the FPGA for the next data collection. The data collection will be triggered once a second based on the 30Hz fiber input (to stay synchronized with the accelerator BPMs). When the accelerator is in pulsed mode, data will only be collected immediately following the Beam Sync fiber input trigger so that the pulsed position is valid. Part or all of the position calculations could be moved from the IOC to the FPGA if needed for real-time processing. This should be avoided as it will take many FPGA resources and limits the flexibility of having the raw data at the IOC/EPICS level. The details of the difference-over-sum based position calculation will be defined by Richard Jones. Each gain setting will require unique calibration constants. An automatic gain switching routine will most likely be implemented but will have the option to be turned off. Temperature related gain drifts will show up in the calculated position so the electronics should be characterized (especially the PMT-5R amplifier). It may be advantageous to include temperature sensors on the Amplifier Power & Control, Splitter and Receiver boards.

A female 37-pin D connector will connect to the Collimator Splitter chassis with 24 TTL amplifier gain outputs (3 per channel) and 8 local/remote TTL status inputs (1 per channel). FPGA registers will be written to and read from EPICS to control the amplifier gains and monitor the local/remote switch statuses. 4 diagnostic DACs, 1 diagnostic ADC and various digital I/O will be included for monitoring/ troubleshooting internal FPGA DSP algorithms and/or support future functionality (lock-in, triggering, position outputs, …). The fiber optic fast feedback output will stream collimator data to the fast feedback system. The tentative plan is to constantly send the 8 digitized and filtered collimator signals and have the fast feedback IOC turn them into the needed positions. It may be possible to send processed position data if the overall control latency is not larger than 150 μs. This would entail the IOC collecting data, calculating a position then writing it to the FPGA for transmission to the fast feedback system (unless the calculations are done in the FPGA).

This document was based on the following meetings:

1/14/2013, Attendees: T. Larrieu, R. Jones, A. Somov, A. Hofler, T. Whitlatch, T. Satogata, M. Spata, J. Benesch, S. Higgins, A. Freyberger, P. Kjeldsen, M. McCaughan, M. Bickley, B. Bevins, O. Garza, P. Francis, J. Musson, T. Allison

2/5/2013, Attendees: T. Larrieu, B. Bevins, A. Somov, I. Senderovich, H. Egiyan, S. Higgins, J. Musson, T. Allison, P. Francis, R. Jones