12GeV Trigger meeting notes:

6-September-2013: C. Cuevas, A. Somov, N. Nganga, H. Dong, W. Gu, J. Wilson, B. Raydo

16 August 2013: C. Cuevas, A. Somov, N. Nganga, H. Dong, W. Gu, B. Moffit

26 July 2013: C. Cuevas, A. Somov, B. Raydo, S. Kaneta, J. Wilson, H. Dong, W. Gu, B. Moffit

19 July 2013: C. Cuevas, A. Somov, H. Dong N. Nganga, B. Raydo, S. Kaneta, J. Wilson, E. Jastrzembski

12 July 2013: C. Cuevas, A. Somov, H. Dong N. Nganga, B. Raydo, S. Kaneta, J. Wilson, E. Jastrzembski, B. Moffit

5-July-2013: No meeting

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1. Trigger/Clock/Sync – TI/TD

6-Sept-2013

→Firmware revisions continue with latest feature of presetting the number of readout 'blocks' that will automatically stop a run.
→We still have plans to setup the final TS and Global crates in the Hal D CH. All the required boards will configured and tested in the CH before moving them to the hall. There are effectively two TS/Global crate test setups now with one in F117 and the EEL109 lab. I imagine the Trigger test stand will be located in the CH once operations begin.

16-August-2013

→TS boards received, tested and delivered to the hall groups.
→One of the production TS boards is in the Hall D CH and this trigger crate can be populated with SD and TD as needed. We will keep the two trigger crates in EEL109 for a while longer to continue with GTP → TS testing.
-->TIM boards have been assembled and tested. These units are delivered to the Hall groups.

26-July-2013

→Small issue with assembly kit in that one of the resistors was 10K rather than 100 Ohm.
→8 RTM boards are in assembly at Sierra

19-July-2013

→Assembly kits have been sent to the CM for the production TS boards.
→RTM boards and kits have been sent out also.
→No significant issues with the testing in the Hall D CH so far.
→TI Master boards have been configured, tested and distributed to the hall groups.

12-July-2013

→TS production boards are on schedule.
→Rear transition boards have been received. These boards can be assembled here, and are the interface between the Densi-shield cables from the GTP.
→No update on the final firmware changes that will be needed for the initial Hall D commissioning.

1. SUB-SYSTEM PROCESSOR (SSP)

6-Sept-2013

→No questions from the uMegas group regarding the SSP.
→The Hall B RICH detector proposal relies on several SSP to readout and control the front end readout chips for each MAPMT. The review went well and Ben had provided significant information for the previous internal review on the DAQ system.
→Documentation for the SSP continues and the additional trigger processing modes have been finished also.
→The MicroMegas group has received the SSP and other hardware needed to continue their R&D with the GEM detector readout.

16-August-2013 (Ben's update below)

→Hall D Firmware is complete:
1) Trigger processing modes:
   a) summing fiber 0-7 (any combination) and reports to GTP
   b) pass-through fiber x to GTP (for single crates used on SSP that pass directly to GTP)
2) VME firmware update (5.5MByte image):
   80 seconds to program time, 15 seconds to verify
3) Monitoring functions
   a) scalers on I/O
   b) Hall D specific pulse integral histograms
   c) serdes bit error monitoring, raw data/waveform capture, data crc

Driver:
I've got a Linux/VxWorks driver that configures the SSP that will be a helpful place for the Bryan to work with so it shouldn't take him long to get it up to par to work with along with CODA.
Documentation:
I'm working on this today and should be completed by end of day...
→SSP firmware (registers) are complete and will need to be given to Bryan for development of the CODA library.

26-July-2013

→Development work is progressing

→Micromegas? No news is good news, and some work has started with using an embedded controller within the SSP.

19-July-2013

-->Firmware development progresses and new features for scalers will be added. There will be CODA driver work to be completed also, but this work will need to be done anyway.
→Configure the Hall D global trigger crate in EEL109 with 8 SSP and the production GTP.

12-July-2013

→Supporting Alex and the Hall D global test stand testing. Alex has two of the pre-production CTP and a single SSP. Plenty of development work in progress.
→Hall A will receive their SSP in the near future. Not a priority, but Ben will deliver a board soon.

2. CUSTOMERS

6-Sept-2013

→Mode 6 TDC for the PCAL is being used. There are a few issues with the data quality that have come into question by Sergey and other Users. Apparently there are issues with the TDC function and improper timing data is recorded when initially running Mode 6 with the PCAL

cosmic setup. Sergey B. has discussed the issues with Ed and Hai. Hai suggests to run Mode 7 to analyze the raw data along with the TDC information.

16-August-2013
→Hall B PCAL group will begin detector tests with the new Mode 6 firmware. After that the FTOF group will use the boards.
→Activity to repair the broken FADC250 production boards has started.
→SBC has been approved to send to CEA Saclay!!

26-July-2013
→Detector groups will use FADC250 with the new "Mode 6" to verify the operation.
→Discussion about pedestal method for "Mode 6" and the ability to change modes within a run.

12-July-2013
→Still waiting for DOE approval to send the SBC to CEA Saclay.
→PCAL for CLAS12 will be testing the new Mode 6 firmware for the FADC250 board. TDC and pedestal information is captured for every pulse and is included in the data stream as Vmin.

3. "B" Switch - Signal Distribution Module (SD)

6-September-2013
→Nick confirmed that the phase clock difference on start up for different crates is the same. The number of times for turning on the crates is low, but the Silicon Lab PLL operation states that the clocks will be in phase. Additional statistics are not needed and these tests are enough to verify that the PLL turn on state agrees with the datasheet specification.

16-August-2013
→Nick has a brief presentation on PLL testing. Results and test setup were presented and the difference in jitter was understandable. Further discussion let to another test plan to measure phase difference on start up for the front end crates. Use 31.25MHz as the test case because this phase difference may be important for the F1TDC crates.

19-July-2013
→PLL testing firmware is still in progress. We will have to coordinate which crate to use for this PLL test.

12-July-2013
→PLL testing in progress.

4. System Diagrams/Fiber Optics

6-Sept-2013
→Elliott would like to combine the Ethernet fiber with the Trigger fiber order for installation in the hall by October. There are many cable trays that still need to be installed before final cable length measurements can be given to the selected vendor.

14-June-2013
→Create a PR and the goal is to submit a purchase order before the end of FY13!!
15-Mar-2013
→No action until cable trays are installed in the halls.
8-Mar-2013
→No report.
8-Feb-2013

→Patch panels and patch cables are being checked in now, and will be distributed to the hall groups
→START procurement for trunk cables in D and B by May??

5. Global Trigger & Trigger Distribution Testing

6-Sept-2013
→Ben is using the production GTP to develop firmware for the CLAS12 tracking trigger. This development will establish experience with the GTP project left over from Scott.
→Low level firmware code has been evaluated/changed by Ben and will continue. Higher level framework from Ben can now be used for the GTP developments.
→Project outline has been drafted by Ben to recruit Chris Hewitt (HPC group) to port an embedded processor on the GTP using Nios. More details will follow, and this could be used for other projects.

16-August-2013
No report.
26-July-2013
→Focus has been the 5Gbps testing with a full crate of FADC250 boards.
→All GTP documentation is wrapped up and plenty of testing remains (Ben).
19-July-2013
→A few I/O ports still need to be functionally tested.
→Densi-shield cable test should be completed with the production TS.
→16 payload board test for 5Gbps has been built. We can use one of the crates to perform this test and characterize the backplane and check BER. There are a significant number of parameters that Scott's firmware will measure and record.

12-July-2013
→DC power testing is complete for both boards!
→Complete functional testing is progressing well.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

6-Sept-2013
-->26 of 33 have been delivered with 8 of the 26 not passing Hai's acceptance test. We will have a phone conference with MTEQ to find out when the last 7 boards will be delivered, and to discuss assembly issues with the boards that did not pass testing.
→Only the 1st article CTPV2 board has passed the FCAT test. Bryan is very busy and the 18 boards that have passed should be run through the FCAT asap.
→There is a long range plan to setup and run the FCAT in EEL109.
→The front panels will be delivered soon.

16-August-2013
→We have a total of 6 production boards with one issue so far on one of the boards. (Clock to U1)
→4 boards can be tested with FCAT and the 1st article production board has already passed the FCAT test.

→Expect delivery of production boards every week until all 32 boards have been received. Vacation plans will stop acceptance testing. Acceptance testing is highest priority.

26-July-2013

-->VME firmware download routine has been completed. This has been tested only in the local test stand crate. Will need to verify on another crate.
→Production CTPv2 passed FCAT testing!

19-July-2013

→All indications from the PCB and assembly companies are positive so we expect the CTPV2 boards to meet the delivery schedule.
→Automatic testing firmware and remote firmware download routines are complete. Hai is documenting the test routine procedure for the acceptance testing activities.

12-July-2013

→Remote firmware download is 95% complete. All other acceptance test firmware is ready for the production boards.

***ACTION ITEMS*: Next meeting - Friday 13 September 2013 @10:30AM in TBA**