Proposed Software Quench Detector Scheme

PXI System Changes:

- The current heartbeat signal from the PXI to the PLC will change from 1Hz to 10Hz
- A Voltage Tap Data Acquisition loop running status bit will be added to the data being sent to the PLC and will be monitored at the PLC scan rate. This bit will be high if only if the voltage tap data loop is running properly.
- An Error bit from the data acquisition loop will also be added to the data being sent. The bit will be low during normal running conditions.

    - The PLC will check for the following PXI condition on each scan:
        - Every .1 seconds the heartbeat will flip from 1 to 0 AND the Status Bit is high AND the Error Bit is low.

        NOTE: Status and Error bits will are updated at .002 seconds.

- PXI Testing:
    - The PXI watchdog will be tested by turning off power to the PXI chassis and monitoring the Fast Dump signal at the PLC.
    - The PXI status bits will be tested by stopping the data acquisition loop with the PXI still online and monitoring the Fast Dump signal at the PLC.

PLC System Changes:

- The PLC heartbeat to the hardware watchdog timer will be changed from 5 seconds ON, 1 second OFF to 10ms ON, 10ms OFF.
- The PLC quench detector code runs much faster than the timer so I will send a tag from the timer through the Voltage Tap algorithms. I will then SUM the Voltage Tap outputs and make a new tag that will be sent to the hardware watchdog. If any of the Voltage Tap instructions fail to execute the output tag will not toggle properly and a Fast Dump will result.

- PLC Testing:
    - The PLC watchdog will be tested by writing a constant to each of the Voltage Tap algorithms separately which will stop the output tag from toggling properly and a Fast Dump signal will be initiated.