Parsing DIRC EVIO

```
============================================================
Event: 4
DDIRCTDCHit:
 rocid: slot: channel: itrigger: dev_id: ievent_cnt: channel_fpga: edge: time:
------------------------------------------------------------------------------
    92     3       0         4       0          4            0     1   261
    92     3       0         4       0          4            0     0   314
    92     3       0         4       0          4            0     1   765
    92     3       0         4       0          4            0     0   818
    92     3      64         4       0          4           64     1   259
    92     3      64         4       0          4           64     0   310
    92     3      64         4       0          4           64     1   763
    92     3      64         4       0          4           64     0   814
    92     3     128         4       0          4          128     1   262
    92     3     128         4       0          4          128     0   317
    92     3     128         4       0          4          128     1   766
    92     3     128         4       0          4          128     0   821
    92     3     256         4       1          4            0     1   260
    92     3     256         4       1          4            0     0   312
    92     3     256         4       1          4            0     1   764
    92     3     256         4       1          4            0     0   816
```

Crate

SSP board 3-5

SSP Unique Channel 0-8128

FPGA board 0-31

FPGA channel 0-191

Time (ns)

Leading = 1
Trailing = 0