12GeV Trigger meeting notes:

25-October-2013: C. Cuevas, B. Moffit, E. Jastrzembski, W. Gu, B. Raydo, H. Dong, N. Nganga

18-October-2013: No meeting

11-October-2013: C. Cuevas, J. Wilson, B. Moffit, E. Jastrzembski, W. Gu, B. Raydo, A. Somov, H. Dong

4-October-2013: Cancelled (Hall D Collaboration meeting)

27-September-2013: C. Cuevas, A. Somov, W. Gu, B. Raydo, B. Moffit

13-September-2013: C. Cuevas, A. Somov, N. Nganga, W. Gu, B. Raydo, E. Jastrzembski, B. Moffit

6-September-2013: C. Cuevas, A. Somov, N. Nganga, H. Dong, W. Gu, J. Wilson, B. Raydo

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1. Trigger/Clock/Sync – TI/TD

25-Oct-2013

→Discussion started regarding the fiber port mapping and new requirements for information between CTP->SSP and TI->TD that define the port map and crate ID. This type of information is not presently in the communication link between CTP→SSP nor TI->TD.

→I believe there has been some discussion with Alex regarding the definition of each trigger bit. Some discussion started about asynchronous triggers, but I did not record good enough notes. What input bits will be considered asynchronous? Or will all inputs to the TS be considered asynchronous?

→William has delivered the TD and TS boards to the Hall D group. The TD boards use the geographic pins from '64x so there is no need to set addressing switches. The fiber transceiver ports for each TD will be populated, so in principle the TD→TI links can be arranged from left to right, and top to bottom. Detector subsystem front end crates (TI) will be assigned to the TD slot and port number.

11-Oct-2013

Discussion about configuring TS/TD crate and GTP/SSP crates in EEL109.

Need to detail a port map for the TD and SSP fiber transceivers. Fiber drawing exists and will be updated soon.

27-Sept-2013

-Bryan has setup the DAQ wiki with a collection of the latest DAQ/Trigger board documentation.

- I noticed that the "User manuals" for the CTP and FADC250 boards need updating.

-Discuss the PEER application,

13-Sept-2013

-->Discussion on firmware updates started,,

→Good progress on latest features for TS.

→Good discussion on board user manuals, and we should have the DAQ group area hold the latest versions. This way we do not have six different sites with six different versions.

6-Sept-2013

→Firmware revisions continue with latest feature of presetting the number of readout 'blocks' that will automatically stop a run.

→We still have plans to setup the final TS and Global crates in the Hall D CH. All the required boards will be configured and tested in the CH before moving them to the hall. There are

effectively two TS/Global crate test setups now with one in F117 and the EEL109 lab. I imagine the Trigger test stand will be located in the CH once operations begin.

1. SUB-SYSTEM PROCESSOR (SSP)

25-Oct-2013
SSP fiber port map is determined and the boards can be configured in the crate. I believe the TI and SD are already in the EEL109 crate and presumably the CPU (roc) will be configured and provided by the Hall D folks.

11-Oct-2013
→The SSP/GTP crate for Hall D will need to be configured and tested within the next few weeks because the crate will be moved to Hall D by the end of October. Ben will need to setup this crate and configure the SSP/GTP boards for initial operations. The fiber optic ports will need to be updated on the Hall D fiber optic distribution drawing. There will be plenty of labeling to be created soon too.
→We briefly discussed the VCSEL safety issues. There will be labels that identify the fiber patch panels to have laser hazard. We need review the laser power levels from these transceivers and document the potential hazards before the readiness review.
→No news from the MicroMegas group.

27-Sept-2013
→SSP is effectively complete and there are a few specific items that will need development for the global 'window' feature and other applications.

13-Sept-2013
-->Documentation and firmware is complete for the Hall D firmware revision.

6-Sept-2013
→No questions from the uMegas group regarding the SSP.
→The Hall B RICH detector proposal relies on several SSP to readout and control the front end readout chips for each MAPMT. The review went well and Ben had provided significant information for the previous internal review on the DAQ system.
→Documentation for the SSP continues and the additional trigger processing modes have been finished also.
→The MicroMegas group has received the SSP and other hardware needed to continue their R&D with the GEM detector readout.

2. CUSTOMERS

25-Oct-2013
Mode 6 testing continues.
11-Oct-2013
→Some discussion and work by Ed regarding the Mode 6 firmware. The plan is to use the playback feature to build pulse waveforms and test the timing algorithm code. There is no need to create a pulse from a function generator for the front panel, and the high resolution timing algorithm can be tested with waveforms created by the playback feature. Using the playback feature, almost any pulse waveform shape can be created to test the timing algorithm. Ed will need to modify control FPGA firmware to use Trig1 to generate Trig2 internally for testing this problem in the lab.
→Priorities for new firmware remain almost the same as the list below. The Pair Spectrometer trigger algorithm may need development sooner than the TOF application.

27-Sept-2013
→Priorities:
CTPV2 testing
Mode 6 repair
Tagger Hit bit application
BCAL cosmics
TOF application
Pair Spectrometer

6-Sept-2013
→Mode 6 TDC for the PCAL is being used. There are a few issues with the data quality that have come into question by Sergey and other Users. Apparently there are issues with the TDC function and improper timing data is recorded when initially running Mode 6 with the PCAL cosmic setup. Sergey B. has discussed the issues with Ed and Hai. Hai suggests running Mode 7 to analyze the raw data along with the TDC information.

3. *"B" Switch - Signal Distribution Module (SD)*

25-Oct-2013
→New SD→TI link firmware 1.0 is ready for testing. 20Mbs is the expected upper limit for this link. (Single pair uni-directional)

11-Oct-2013
→Nick and William can work on the SD→TI link firmware. This is a good project but definitely a lower priority than other jobs. Has the link function been defined?

13-Sept-2013
→The job is never done till the paperwork is complete.
Only a few items need to be updated. The 31.25MHz clock will be used for the F1TDC boards and there is a minor issue with the setup of the SD PLL.

6-September-2013
→Nick confirmed that the phase clock difference on start up for different crates is the same. The number of times for turning on the crates is low, but the Silicon Lab PLL operation states that the clocks will be in phase. Additional statistics are not needed and these tests are enough to verify that the PLL turn on state agrees with the datasheet specification.

4. System Diagrams/Fiber Optics

25-Oct-2013
→Drawings are at the final draft state and 4U fiber patch has been delivered. Still need to measure the length of the trunk line routing. A visit to the hall weekly shows interesting progress for many detector systems, but many cable trays and other racks are not in place.
→Trunk fiber order is 5-7 days ARO, from Richmond, so it should not take long to hook up after we receive the cable.

11-Oct-2013
→Fiber drawings will need update but good thing the system was already in the advanced planning stage. Vendor for trunk line cables has been identified and hopefully procurement will allow the use of this vendor, otherwise delays will occur.
→Some discussions after the meeting regarding the fiber port map assignments for the TD and SSP boards. It may make sense to skip a slot in both the Global and TS crates to make the fiber cable spaghetti less of an issue.

→Still need to measure the length of the trunk lines and we can go to the Hall soon to pull the tape measure. The "Online Data Challenge" test requires a dozen front end crates, and the BCAL sub-system is the perfect candidate considering the fiber trunk lines are fairly short and more accessible than other cable tray routes.

27-Sept-2013
Meeting with Tim and Tom in the hall to review the cabling needs for the trigger fiber optics. There are still many racks and trays that are not installed. As soon as these trays are installed I can measure the lengths as a first approximation and complete the PR.
Nov 1

6-Sept-2013
→Elliott would like to combine the Ethernet fiber with the Trigger fiber order for installation in the hall by October. There are many cable trays that still need to be installed before final cable length measurements can be given to the selected vendor.

5. Global Trigger & Trigger Distribution Testing

25-Oct-2013
→Chris Hewitt can begin work for the embedded Linux on the GTP.

27-Sept-2013
→Same notes as last time,

6-Sept-2013
→Ben is using the production GTP to develop firmware for the CLAS12 tracking trigger. This development will establish experience with the GTP project left over from Scott.
→Low level firmware code has been evaluated/changed by Ben and will continue. Higher level framework from Ben can now be used for the GTP developments.
→Project outline has been drafted by Ben to recruit Chris Hewitt (HPC group) to port an embedded processor on the GTP using Nios. More details will follow, and this could be used for other projects.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

25-Oct-2013
→Hai has completed the remote firmware download work and this new code has been tested. There are several CTPV2 boards that have already passed the FCAT but the latest firmware will have to be loaded. For completeness, the CTPV2 boards should be tested again in FCAT.
→12 production CTPV2 boards were delivered to MTEQ on 8-Oct and 6 were returned on 15-Oct. 2 of the reworked boards pass the acceptance testing, and the remaining do not and will have to be returned for rework(reball?). The remaining 6 boards have not been received yet, but should be at JLAB the week of 28-Oct-13.

11-Oct-2013
-->Hai and Jeff made successful political connections with folks at MTEQ regarding the rework issues. 12 boards delivered to MTEQ and detailed repair discussions were held. No surprises

and the confidence level is high for the non BGA/LGA device repairs. Hopefully no re-ball work is required.

27-Sept-2013

→All boards are on site. 20 boards pass acceptance testing. 10 boards of 33 boards will need minor rework/repair and will be sent to the assembly vendor next week.
→Will begin using the eel FCAT to test the boards that passed Hai's acceptance testing.
→CODA library work will be needed to include the remote (VME-TI) firmware download.

6-Sept-2013

-->26 of 33 have been delivered with 8 of the 26 not passing Hai's acceptance test. We will have a phone conference with MTEQ to find out when the last 7 boards will be delivered, and to discuss assembly issues with the boards that did not pass testing.
→Only the 1st article CTPV2 board has passed the FCAT test. Bryan is very busy and the 18 boards that have passed should be run through the FCAT ASAP.
→There is a long range plan to setup and run the FCAT in EEL109.
→The front panels will be delivered soon.

16-August-2013

→We have a total of 6 production boards with one issue so far on one of the boards. (Clock to U1)
→4 boards can be tested with FCAT and the 1st article production board has already passed the FCAT test.
→Expect delivery of production boards every week until all 32 boards have been received. Vacation plans will stop acceptance testing. Acceptance testing is highest priority.

ACTION ITEMS: **Next meeting - Friday 1-November 2013 @10:30AM in L210A**