12GeV Trigger meeting notes:

3 June 2011: C. Cuevas, S. Kaneta, J. Gu, B. Raydo, B. Moffit, A. Somov, J. Wilson, .F. Ahmed, N. Nganga. E. Jastrzembski

27 May 2011: C. Cuevas, H. Dong,S. Kaneta, J. Gu, B. Raydo, B. Moffit, A. Somov,

20 May 2011: C. Cuevas, S. Kaneta, J. Gu, B. Raydo, J. Wilson, B. Moffit, N. Nganga, E. Jastrzembski

13 May 2011: C. Cuevas, N. Nganga, S. Kaneta, J. Gu, A. Somov, B. Raydo, J. Wilson, B. Moffit

6 May 2011: C. Cuevas, N. Nganga, S. Kaneta, J. Gu, A. Somov, B. Raydo; H. Dong

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0. Trigger/Clock/Sync – TI/TD

3 June 2011

→Assembly quotes are expected soon to build 12 boards and the part kits are almost 100% complete. The front panel material has been ordered but not received, and machining the panels will occur as soon as the material is received.

→Testing in the lab with two crates is going well and there are a few issues with the timing delay recorded during two crate testing. The transition time from receiving a trigger signal from the SSP to the time the SD Trig1_Out occurs appears much too long. William will investigate.

27 May2011

→The circuit board order for the pre-production units has been awarded. The components are on site and once the bare boards have been received and verified, they will be sent to the assembly vendor. Presumably all the front panels have been completed for the pre-production quantity.

→The TI can be tested with the existing FADC250-V2 to measure and record the maximum sustainable trigger rate in conjunction with the front end BUSY signal to verify the proper operation of the TI under maximum specified conditions. Multiple signals can be applied to the two FADC250 units to produce front-end data for readout.

20 May 2011

→Pre-production parts have been received. Assembly quotes ready. Final Gerber check in process.

→William presented summary of TS meeting that was held on Monday 16-May. File is located on the trigger wiki page.

13 May 2011

→Pre-production parts on order, fabrication files ready, PR can be started and after initial test of multiple FADC250 the order will be placed.

→Both TI boards have been configured in the EEL109 test setup for a few weeks. Not sure if these units have been run continuously for a full shift to verify that the values of counters in both units for trigger, clock, etc match perfectly. Trigger signals through the fiber distribution to each crate have been de-skewed.

6 May 2011

Two FADC250V2 boards are installed in one crate. Some issues with token passing in block transfer mode. Need to check this early next week. What is the token passing sequence? i.e. TI always initiates the token in block mode?

2. ***SUB-SYSTEM PROCESSOR (SSP)***

3 June 2011

→Ben and Hai have completed and implemented the firmware that manages the trigger data stream from the CTP to the SSP. This firmware has been has been tested and works with two crate test station!! Significant milestone!!! Pre-production order before end of fy11?

→ We discussed a pre-production order of SSP before the end of fy11, but it is not clear if this is the best approach. There are not many detector tests in the next year that drives the need to produce the SSPs at this time. There are minor changes to the prototype, and it makes more sense to review the design and proceed with pre-production quantities in the first quarter of FY12.

27 May 2011

Ben and Hai have installed and initially tested the firmware used in both the CTP and SSP for serial transport of trigger information. Ben showed a ChipScope plot of signal received from a single CTP which was the sum of two channels, one signal into each FADC250. It is a perfect opportunity to measure and record the serial transport time for each of the modules in the system. This transport time will be fixed for each "link" (i.e. FADC250 to CTP and CTP to SSP) but needs to be measured and recorded.

20 May 2011

→New communication link from the CTP to the SSP has been discussed and implementation plan is in the works. It will be important to measure and record the propagation through the SSP. Two CTP will be implemented with Ben's firmware, and then the CTP->SSP link will be tested. SSP VME control/configuration registers will be defined soon and the command map will be distributed. Diagnostic 'history FiFo' can be implemented later.

13 May 2011

→ Ben and Hai have discussed the link definition that will be used for the two crate test. Ultimately, the SSP will collect the summing information from both CTP and generate a trigger signal that will drive the TI running in TS mode. There will not be a need for complex functions on the SSP, but a few registers will be needed to monitor the trigger output rate, and set the final threshold for the two crate sum.

→ECO list will need to be applied to the schematic and board layout as time permits.

6 May 2011

CTP → SSP link is the next work. Discussions have started. ECO list is documented but not implemented in schematic or pcb. We may want to purchase high cost components this fiscal year for the production quantity if funds are available.

3. CUSTOMERS

3 June 2011

→38 FADC250-V2 preproduction boards have been returned to the manufacturer for test verification. If no problems are found, then we must decide how to proceed with the assembly.

→We have three fully functioning FADC250-V2 boards and two will remain dedicated to the two crate test station. There are many tests to configure and measurements to record to fully qualify the performance of the system to meet or exceed specifications.

→The third board may need to be 'time-shared' with Hai/Ed and Fabian until we receive the next assembly batch.

27 May 2011

→An issue with the preproduction bare boards has been discovered and this will impact the delivery schedule of the remaining 33 assemblies. The bare boards will be sent to the board manufacturing company for test verification. Stay tuned,,,

13 May 2011

→There is another small order of 4 FADC250-V2 for the Radiation Detector Group and the Injector Group. This assembly order will be released in a week as soon as the bare boards have been received for the pre-production order.

→There are several groups that will need to begin testing detectors soon, and they will need crates, FADC250, SD, and TI. The need to order TI and SD will be urgent in a few months.

4 "B" Switch - Signal Distribution Module (SD)

3 June 2011

→ Documentation of the PLL phase adjustment method including test results and scope photos is a work in progress. The existing implementation method to adjust for precise clock phase used Nios as the embedded micro-controller code to perform the phase adjustment technique. The Altera Cyclone III part is currently at 50% resource usage and there are no issues with this part for the preproduction run.

→Preproduction:

ECOs to schematic have started, and will need to be implemented on the PCB routing. We have had the parts for six more boards for several months, and price estimates for bare board and circuit assembly need to be received soon.

27 May 2011

→Nick is at another meeting and will need to implement ALL Engineering Changes to the schematic and PCB and prepare for a pre-production order. The test stand group will need the 2nd SD during the week of June 1 to complete a two crate test with a single FADC250-V2 in each crate.

→Complete diagrams and documentation for the phase adjustment technique that was successfully implemented using the Altera Nios and carry chain logic.

20 May 2011

→Token passing is OK!

→Diagrams for the phase adjustment technique will be produced. Successful implementation

→Turn-Key Production order discussion.

13 May 2011

→Nick has successfully implemented the phase adjustment technique on one of the SD. ~100ps is the resolution for measuring the phase difference using a dedicated carry chain circuit on the Altera FPGA. The full loop control has been tested through SPI to the Silicon Lab PLL.

→Only one SD board has been modified and only one needs this change at the present time.

→ECOs must be completed in the schematic and circuit board as soon as possible and the parts kit for ordering six more SD assemblies is virtually complete.

6 May 2011

Phase adjustment technique with Altera FPGA. Any progress?

Carry chain technique to measure phase difference and feed correction through SPI interface to the PLL chips.

We have a plan to use the Silicon Lab board and the old TI prototype to implement a test of the new phase compensation technique. Done by Wed 11-May-2011. B. Raydo will assist.

5. System Diagrams/Fiber Optics

3 June 2011

No report. Fiber specification is due soon for pre-procurement plan.

27 May 2011
There have been good discussions with Sergey et al from CLAS12 to work on displays and other GUI for configuration and control of the plethora of functions from the trigger modules. The CLAS12 folks would certainly like to get started with their detector DAq testing and as soon as we have completely verified the FADC250 assemblies, and tested them in a full crate, groups can begin their detector tests.

20 May 2011
GUI and displays for graphing results from test stand modules. How are we going to implement this, what values need to be displayed? What scaler items need to be implemented?

Global SUM plot—Read from SSP (Could read CTP1 and CTP2 from SSP also)
Crate SUM plot – Read from CTP (Via I^2C)
Scalers: A strong comment from Bryan Moffit: Put the scalers in registers, NOT data stream. Must create a list of scaler registers to implement in the hardware.

Event counters
Trigger counters
Clock counters
Readout rate Vs trigger rate
Channel bar graphs
Any channel 'Scope shot'

13 May 2011
→No report on fiber specification draft document.
→16 more VXS crates arrived and will need preliminary checkout soon.
→EEL109 two crate test station has new Wiener VXS crates installed!

6 May 2011
No report.

5. Two Crate DAq test configuration

3 June 2011
→ ***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

→ Ben presented a few oscilloscope photos and Chipscope plot from the SSP. The SSP plot clearly shows the two signals that were injected into each FADC250. One signal was delayed by 15ns and the SSP 'history' plot shows these signals clearly. There are several small issues to clean up with how the SSP handles the data bytes from the CTP, but it appears that the hardware is working and is ready for further testing.
→ There was a discussion on how the DAq was configured, i.e.) Handshaking, and what run mode was configured? It appears that the system was operated in non event 'blocking' mode. The trigger count matches from each module in a crate, but the trigger count information crate to crate do not match. What is the difference? Why?
→ No Token passing scheme was used during the single FADC250/crate test but 2eSST used for readout.
What is the BUSY 'high water' threshold setting?
→ Issues:
Synchronization MUST have this working flawlessly for high rate testing.
Data integrity , Need some Data plots to show trigger rate Vs readout data size.

Comparison tables for 'scalers' for a each module within a crate and comparisons between crates: Trigger count from each board, Busy counter? Other?

27 May 2011

We have three FADC250-V2 boards that are working and will proceed to configure the two crate test stand with one FADC250-V2 per crate. Will need the 2nd SD board and will also use the SSP to collect trigger data from each crate trigger processor. We will measure and record the trigger transition delays (Should be fixed and is a function of the Aurora serial protocol) from each serial link.

13 May 2011

Four FADC250-V2 boards are in the EEL109 lab!! Two of the boards were received 12-May-2011 and will need to be tested with Hai's automatic test routine.

Next Steps:
Install two FADC250-V2 in one crate
"Hardcode" payload ports to CTP
Troubleshoot token passing problem
Set 'Sum' threshold to CTP
Use CTP output to TI(TS) to create final trigger
    Then;
    Install two boards in each crate
    Use hardcoded CTP in each crate
    Use two CTP outputs to drive two TI(TS) inputs to create final trigger
Initial test complete
→Need to create simple 'event' displays to view important values during test procedures

6 May 2011

We should have three or four FADC250V2 boards in the EEL by 13-May-2011. Two crate testing will begin next week with one flash board in each crate.
Good progress by Bryan et al.

22 April 2011

-->Ed and Hai have completed the final firmware revisions for the initial FADC250-V2 boards and at least one unit should be installed in the EEL109 lab for an initial test with the TI and SD module. Continued progress, and it will not be long before we have two full front end crates!
-->The main goals of the two crate test are extracted from past meetings as follows:
The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:
→Goals of the integration testing:
-Verify clock distribution through TID->SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)

-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)

So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).

B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

6. Crate Trigger Processor (CTP)

3 June 2011

→ Two CTP are operating in each of the crates with a single FADC250-V2! Aurora transceiver speed is 2.5Gb/s per lane and the firmware to configure and select the specific payload slot is 'hardcoded' for now. As we add more FADC250s to the crates this will have to be configurable through registers.

→ There was a brief discussion on pre-production of the CTP and similar to the discussion on the SSP, it may be best to review the required changes to the CTP, and then implement the changes for a pre-production order in first or second quarter of FY2012. There are no immediate needs for detector testing that include CTP except for the HPS test proposal. We have four units, and the CTP will require further testing when the crates are full.

27 May 2011
See SSP notes

20 May 2011
Two FADC250V2 have been tested in one crate with a CTP @2.5Gb/s with signals from the front end of the FADC250V2. We are 1/16th of the way there!!! Original version of the CTP is used in this test.

2nd crate will use 2nd original version of the CTP.

→Hai has successfully tested the latest version of the FADC250 boards with the CTP. Presently the CTP is 'hardcoded' to accept serial trigger data from pre-determined payload slots. Not sure how much work it will take to implement a register that will enable/disable a serial stream from a particular payload slot. For the immediate future, the payload serial streams to the CTP will be 'hardcoded'.
→We have 4 CTP units and I am not sure which ones have been exercised with the latest version of the FADC250. The two CTP with the V5FX70T devices will be tested at the higher serial transfer rate (5Gb/s) but this test is not the highest priority and will be delayed.

13 May 2011
Ben has firmware that was developed during testing of the SSP. Re-use code

6 May 2011
Testing has started with the FADC250V2 boards and the CTP. Initial serial transceiver testing will use 2.5Gb/s per lane.

7. GTP and Global Crate Developments

3 June 2011
→ Assembly quotes and board fabrication quotes have been received and are reasonable for ordering two bare boards and building one completely. One board will be a partial build with the power components only. Front panel design can be started now, since component placement is final.
→ Firmware development activities will be full time once boards have been received and sent to the assembler.
--Hardware functional test:
--Aurora transceiver block
--Ethernet
--Processing core
--I^2C block

27 May 2011
→Fabrication files ready to be checked thoroughly and quotes for bare board and assembly have been received. Is the BOM final and do we have all components kitted in the lab? We will need to have another group contribute funds for the prototype, and this is a work in progress. The order for the boards and assembly should pass through procurement without issues, considering Scott has received estimates from several sources.

→Firmware development: Several complex sections:
-Ethernet interface
-SSP serial streams
-Global logic
-Nios implementation

-Functional hardware test is the first plan

20 May 2011

→RFP for circuit board fab and assembly.
→Review schematic: DRC
→Review Gerbers
Large polygons and large smd pads. Do manufactures require thermal relief?
→Parts kits have been prepared and ordered.
→Who's going to pay for the prototype fab cost?

13 May 2011

→Scott is reviewing the component purchase requisitions and the board has been fully routed. Post routing verification is presently underway and it is time to obtain a price quote for at least two bare boards.
→There has been some discussion regarding the Densi-shield connectors and also the timing skews between the output trigger bits. Presently, the GTP drives the 32 trigger output bits from the Altera FPGA via LVDS. These LVDS signals are buffered and drive the Densi-shield connector with pECL level signaling to be received by the TS. These outputs from the GTP will not be 'registered' before being driven to the TS, and the TS will be responsible for latching and de-skewing (if required) the 32 trigger bits.
→Final check of fabrication files will happen soon, so that we can order the boards in a few weeks. One board will be partially assembled for full DC power verification and then a full assembly will be produced.

6 May 2011

16 layer routing is 90% complete. DDR2 memories are the last section being routed and pin swapped. Progress coming along nicely. Need to order parts ASAP and prepare board manufacturing procurements including assembly/solder requisition.
Review schedule and update order date (Milestone)

ACTION ITEMS: **Next meeting → Friday 10 June at 10AM in F226**