12GeV Trigger meeting notes:

17 June 2011: C. Cuevas, S. Kaneta, J. Gu, J. Wilson, . N. Nganga. E. Jastrzembski, D. Abbott, H. Dong

10 June 2011: C. Cuevas, S. Kaneta, J. Gu, B. Raydo, J. Wilson, . N. Nganga. E. Jastrzembski

3 June 2011: C. Cuevas, S. Kaneta, J. Gu, B. Raydo, B. Moffit, A. Somov, J. Wilson, .F. Ahmed, N. Nganga. E. Jastrzembski

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0. Trigger/Clock/Sync – TI/TD

17 June 2011

Assembly quotes received and a few components that were not on the original order have been ordered. After the boards and parts are received the entire 'kit' will be shipped to the assembly vendor. The assembly order is written with a 10 day delivery after receipt of boards and components.

10 June 2011

→Assembly order is for 10 units. No assembly quotes received yet, and a few components need to be ordered to complete the assembly kit. William has a test plan in place once the TI-D boards are received from the assembler. .

→A brief discussion about how many of these assemblies will be configured for full TID mode, because 8 F/O transceivers will be needed for TI-D boards. Most of these units will be configured for single F/O transceiver as TI boards. William will manage the configuration of each unit and keep track of their respective locations.

3 June 2011

→Assembly quotes are expected soon to build 12 boards and the part kits are almost 100% complete. The front panel material has been ordered but not received, and machining the panels will occur as soon as the material is received.

→Testing in the lab with two crates is going well and there are a few issues with the timing delay recorded during two crate testing. The transition time from receiving a trigger signal from the SSP to the time the SD Trig1_Out occurs appears much too long. William will investigate.

2. *SUB-SYSTEM PROCESSOR (SSP)*

17 June 2011

→No report from Ben, but I know he has demonstrated a few nice diagnostic tools that will produce plots of the data stream 'snapshots' from the CTPs and SSP.

-->After most of the two crate test activities have been completed, the focus will be to complete the SSP minor circuit modifications and prepare for a procurement of the quantities needed for Hall D.

10June 2011

-->Ben has completed the modifications to fix the 'endian' issue with the data from the CTP. Diagnostic tools to view incoming data streams have been prepared. Ben has implemented a histogram application in the SSP which can be tested as soon as Bryan has time.

3 June 2011

→Ben and Hai have completed and implemented the firmware that manages the trigger data stream from the CTP to the SSP. This firmware has been has been tested and works with two crate test station!! Significant milestone!!! Pre-production order before end of fy11?

→ We discussed a pre-production order of SSP before the end of fy11, but it is not clear if this is the best approach. There are not many detector tests in the next year that drives the need to

produce the SSPs at this time. There are minor changes to the prototype, and it makes more sense to review the design and proceed with pre-production quantities in the first quarter of FY12.

3. CUSTOMERS

17 June 2011
Two week delivery after Advanced Assembly receives the FADC250-V2 boards from ACE.
July 6th should begin acceptance testing. Move a full size VXS crate to the EEL-109 lab by next week to set up for the acceptance testing.

10 June 2011
→38 FADC250-V2 bare boards were returned to the vendor for re-test. All of the boards have passed re-test, and the one assembly that had a short circuit trace has been repaired.
→Assembly of the remaining 38 boards will resume as soon as all bare boards have been received by the assembly company.
→The single board acceptance test station is ready for the pre-production lot, and once these boards pass acceptance testing they can be installed in the two crate test station.

3 June 2011
→38 FADC250-V2 preproduction boards have been returned to the manufacturer for test verification. If no problems are found, then we must decide how to proceed with the assembly.
→We have three fully functioning FADC250-V2 boards and two will remain dedicated to the two crate test station. There are many tests to configure and measurements to record to fully qualify the performance of the system to meet or exceed specifications.
→The third board may need to be 'time-shared' with Hai/Ed and Fabian until we receive the next assembly batch.

4 "B" Switch - Signal Distribution Module (SD)

17 June 2011
→Implementing all ECOs on the schematics and layout have been completed... Nick has been working on the firmware changes needed to implement the I^2C interface for the new SiLab PLL part. Nick has designed a small sub-circuit board with the new SiLab PLL part and will use the Cyclone III FPGA on the Altium Nano board to verify I^2C code changes.
→Board quotations and assembly quotations have been requested from vendors and the parts kit is virtually 100% complete.

10 June 2011
→Nick showed results from new SiLab part that will automatically phase align the output at the power on state. The new part is virtually a drop in replacement and next week the schematic will be updated. The PCB ECOs will need to be completed soon, and then it is time to order the six pre-production units!

3 June 2011
→ Documentation of the PLL phase adjustment method including test results and scope photos is a work in progress. The existing implementation method to adjust for precise clock phase used Nios as the embedded micro-controller code to perform the phase adjustment technique. The Altera Cyclone III part is currently at 50% resource usage and there are no issues with this part for the preproduction run.
→Preproduction:
ECOs to schematic have started, and will need to be implemented on the PCB routing. We have had the parts for six more boards for several months, and price estimates for bare board and circuit assembly need to be received soon.

5. System Diagrams/Fiber Optics

17 June 2011
→Armen has completed the final draft versions of the CLAS12 trigger system fiber optic cabling drawing. The drawings show all components needed for the installation in Hall B. The fiber patch panels and fiber optic cables will be added to the order for Hall D to reduce the price significantly. The best method will most likely be a phased procurement, because the installation of this hardware will happen about a year later in Hall B.

10 June 2011
→Fiber Optic system diagrams have been started for the CLAS12 installation in Hall B. Fortunately the parts and fiber optic cabling will be the same, but the quantities and lengths of the cables will of course be different.
→***Deadline*** for the Trigger System Fiber Optic specification is 15-July!

3 June 2011
No report. Fiber specification is due soon for pre-procurement plan.

6. Two Crate DAq test configuration

17 June 2011
Synchronization issue needs to be resolved. Counter values match within a crate, but values between the two crates do not match.

Prepare to run a full 8 hour test with 16 out of 32 channels occupied. The trigger rate could be set relatively high, (>25KHz) and the FADC250s could be run in raw data mode and pulse sum mode. Bryan mentions that he will have to come up with a method to 'prescale' the data that gets saved on disk.

Discussion about Busy management and three modes of TS functions. Lock mode, Trig→Trig_ACK, Buffered with a limit, Large Buffer(Full Pipeline)

10 June 2011
→No update or further testing has been documented since last week's initial breakthrough. There are still synchronization issues to be resolved along with a variety of other minor changes that need to be implemented.
→Ben has been working on diagnostic 'tools' that should help to graphically show the trigger rates, and history waveforms for the global sum and global sum threshold level. There are many other plots that would be very useful to verify all boards in the system are functioning properly and progress continues.
→We will not have more FADC250-V2 boards for a few weeks, so the next goal would be to configure the two crates to run for a full 8 hour 'shift' at a nominal trigger rate of let's say 100KHz with at least 16 of 32 channels occupied.
→No discussion on implementing 'playback' mode, but this mode remains a strong option for completely and deterministically testing all the boards in the system.

3 June 2011
→ ***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

→ Ben presented a few oscilloscope photos and Chipscope plot from the SSP. The SSP plot clearly shows the two signals that were injected into each FADC250. One signal was delayed by 15ns and the SSP 'history' plot shows these signals clearly. There are several small issues

to clean up with how the SSP handles the data bytes from the CTP, but it appears that the hardware is working and is ready for further testing.
→ There was a discussion on how the DAq was configured, i.e.) Handshaking, and what run mode was configured? It appears that the system was operated in non event 'blocking' mode. The trigger count matches from each module in a crate, but the trigger count information crate to crate do not match. What is the difference? Why?
→ No Token passing scheme was used during the single FADC250/crate test but 2eSST used for readout.
What is the BUSY 'high water' threshold setting?
→ Issues:
Synchronization MUST have this working flawlessly for high rate testing.
Data integrity, Need some Data plots to show trigger rate Vs readout data size.
Comparison tables for 'scalers' for a each module within a crate and comparisons between crates: Trigger count from each board, Busy counter? Other?

22 April 2011
-->Ed and Hai have completed the final firmware revisions for the initial FADC250-V2 boards and at least one unit should be installed in the EEL109 lab for an initial test with the TI and SD module. Continued progress, and it will not be long before we have two full front end crates!
-->The main goals of the two crate test are extracted from past meetings as follows:
The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:
→Goals of the integration testing:
-Verify clock distribution through TID->SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been

implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

6. Crate Trigger Processor (CTP)

17 June 2011

Schedule review for ECOs and minor revision additions. The Hall D CTPs must be finalized and ordered by end of the first quarter in FY12.

10 June 2011

→The final version of the CTP needed for Hall D is 23 units. This quantity does not include spares. Hall B will require 21 CTP units.

→The four existing prototype CTP units are stable and will meet or exceed Hall D requirements, so the next step is to finalize the minor engineering changes to the board, and add the front panel I/O that has been requested from previous workshops/meetings.

→After the revisions have been completed and verified, we will order the final version with at least two units as first article acceptance.

3 June 2011

→ Two CTP are operating in each of the crates with a single FADC250-V2! Aurora transceiver speed is 2.5Gb/s per lane and the firmware to configure and select the specific payload slot is 'hardcoded' for now. As we add more FADC250s to the crates this will have to be configurable through registers.

→ There was a brief discussion on pre-production of the CTP and similar to the discussion on the SSP, it may be best to review the required changes to the CTP, and then implement the changes for a pre-production order in first or second quarter of FY2012. There are no immediate needs for detector testing that include CTP except for the HPS test proposal. We have four units, and the CTP will require further testing when the crates are full.

7. GTP and Global Crate Developments

17 June 2011
ORDERED! Boards due 6-July
Partial assembly first: Power section
Full assembly after power verification
Firmware:
Ethernet development
Acceptance test firmware to include Ethernet loopback.

10 June 2011
→PR is waiting for account codes
→P0 test cards will be here next week.
→Firmware development is proceeding and the development will be prioritized for the several sections of the design. See detail list from last week.

3 June 2011
→ Assembly quotes and board fabrication quotes have been received and are reasonable for ordering two bare boards and building one completely. One board will be a partial build with the power components only. Front panel design can be started now, since component placement is final.
→ Firmware development activities will be full time once boards have been received and sent to the assembler.
--Hardware functional test:
--Aurora transceiver block
--Ethernet
--Processing core
--I^2C block

ACTION ITEMS: **Next meeting → Friday 24 June at 10AM in F226**