Hall D Online Meeting

31 January 2008

Fast Electronics

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Group Leader
Jefferson Lab
Experimental Nuclear Physics Division

Electronics Plan - Update

FADC250 Update & Test Plans

System Engineering

-- Drawings/Documentation

-- Preparation for Trigger/DAQ sub-system review

“The Electronics Plan”

- GlueX- Doc - 614

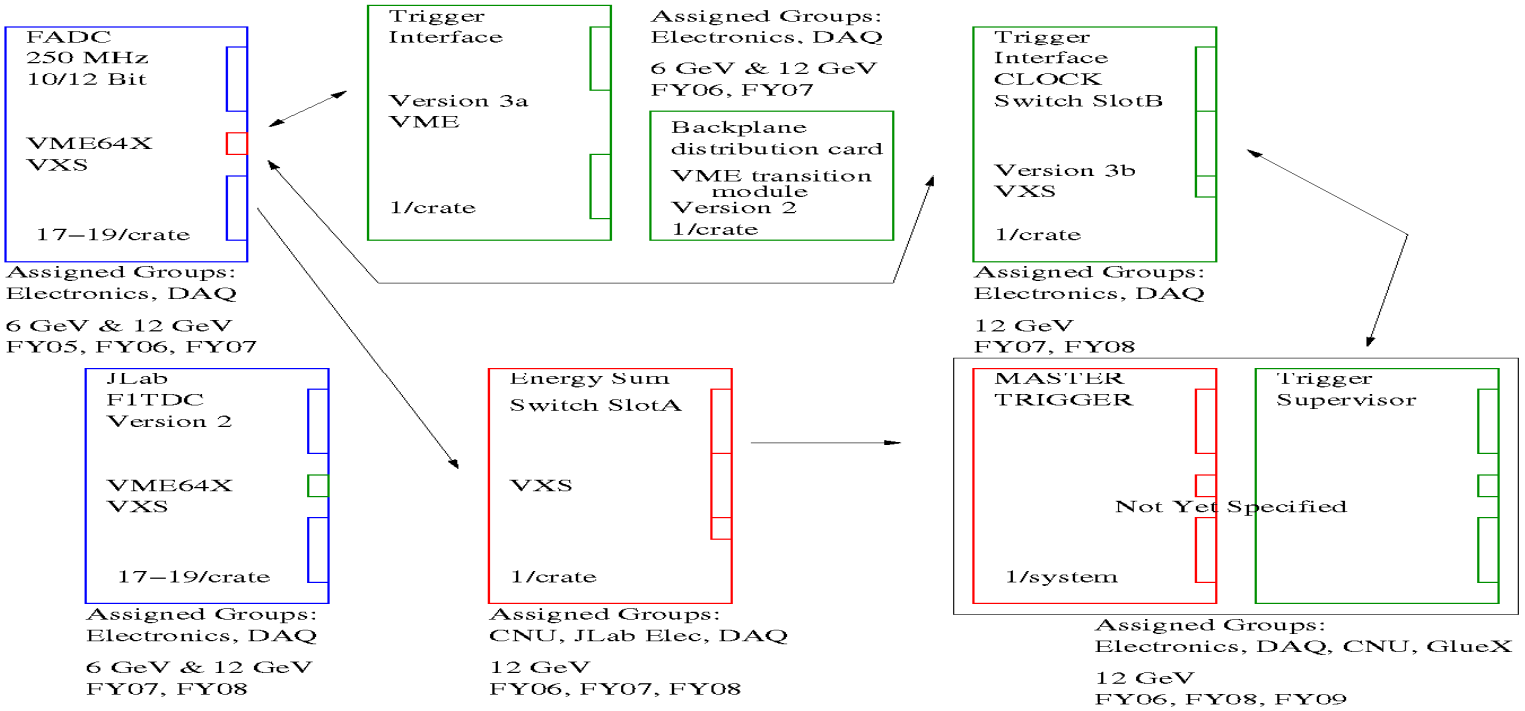
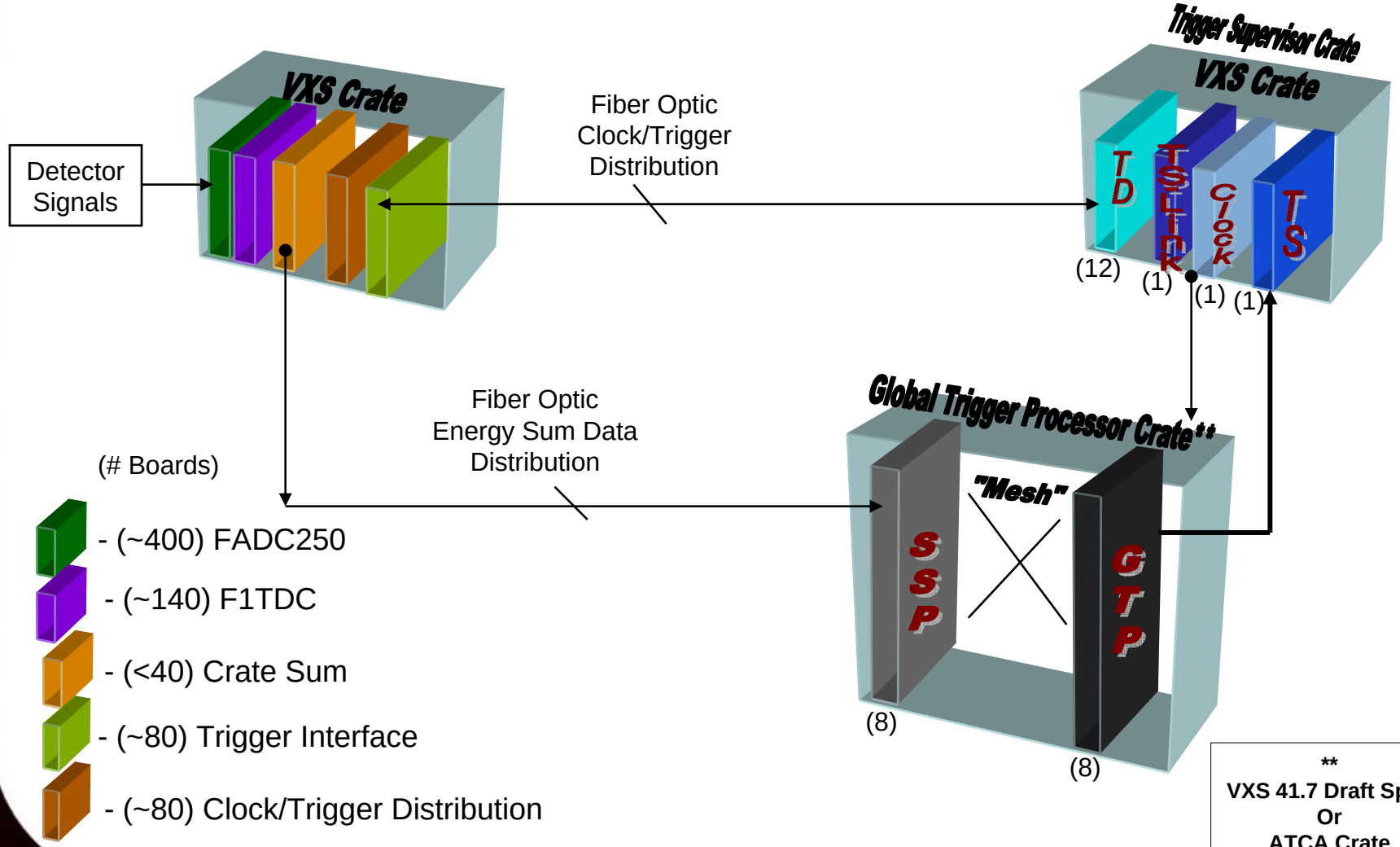


Figure 1: Schematic of the electronic boards that are required to support the plans for GlueX pipeline electronics and data acquisition. Indicated are the module classifications, responsible groups, expected use in the 6 or 12GeV program, and estimate of time frame for design and prototyping.

"Updated Electronics Plan"



Cuevas 31Jan08

Details about the updated plan,,

- 34 weeks until the end of FY08
- We have identified FY09 PED activities that will start now

1. FADC250 work will continue – Need to fabricate four more prototypes
2. 20 Slot VXS crate testing – Qualify new backplane; Tests with multiple FADC250 & TI
3. **Trigger Interface** – Design and fabrication of prototype unit in progress (Ed, Ben)
4. **Clock/Trigger Distribution module** – Welcome Abishek Gupta to Fast Electronics Group
5. **F1TDC Version 2** – Create new specifications and functional requirement document (Fernando, Ed)
6. **Crate Energy Sum module** – Design and prototype circuit board for full crate (Hai, Jeff, Ben, Chris)

- Detailed System Drawings will be completed in February for Trigger/DAQ sub-system review (Chris, Mark)

- Global Trigger Processor crate and conceptual design have progressed significantly
  - Draft Specification for Subsystem Processor (SSP) completed (Ben)
  - Global Trigger Processor – Need Draft Specification (Dave Doughty?,,,)
  - Trigger Supervisor – Need Draft Specification (Ed)
  - Clock/Trigger Distribution – Need Draft Specification (Ben, Ed, Chris,,,)

FADC250 Update and Test Plan

- FADC250 – Meeting every Friday –
  - 5 prototypes built and functional (See Table)
  - Raw data readout mode successfully tested at 250Msps
  - New commercial parts with Gigabit Transceivers working in loop back mode for two week continuously!! Two modules with 3.125Gbps transmission speed, and BitErrorRateTest produces no failures. (Hundreds of Terabits,,)
  - Planning to produce 4 more prototype modules to support test stand development and other essential system tests.
  - Peripheral clock & trigger modules have been designed to support single module testing
  - 12 bit design is on the horizon,,,,

Prototype status: Updated 25Jan08

Board #	ADC Type	VXS	Status Notes	
11089-1-001	10 bit	P0 installed	"Hai's board"	Testing continues
11089-1-002	10 bit	P0 NOT installed	Ed's board	Testing continues
11351-1-001	12 bit	P0 installed	8 channels only	
11351-1-002	10 bit	P0 installed	Received 7Jan08	IBERT SerDes Testing for 2 weeks straight!!!
11351-1-002	10 bit	P0 installed	Received 7Jan08	IBERT SerDes Testing for 2 weeks straight!!!

System Engineering

Hall D Drawing and Document Numbers

Description	**Drawing Number**
Trigger System – Top Level	D00000-16-08-0000
Level 1 Energy Sum – Fiber Distribution	-16-08-0001
Trigger_Link and Clock Distribution – Fiber Optic	-16-08-0002
Specifications & Functional Description	
FADC-250 Module	-16-08-S000
Crate Energy Sum Module	-16-08-S001
Trigger Interface Module	-16-08-S002
Front-End Crate Clock/Trigger Distribution Module	-16-08-S003
Sub_System Processor Module	-16-08-S004
Global Trigger Processor Module	-16-08-S005
Trigger Supervisor Module	-16-08-S006
Trigger & Clock Distribution Module	-16-08-S007
TS Crate Trigger_Link Hub Module	-16-08-S008
TS Crate Clock Hub Module	-16-08-S009
VXS Crate Specification (JLAB Requirements)	-16-08-S010

System Engineering

Hall D Drawing and Document Numbers continued,,

Description	Drawing Number
Readout Controller Network – Top Level	D00000-16-09-0000
High Speed DAQ Subnet– Fiber Distribution	-16-09-0001
Slow Controls Subnet -- Ethernet	-16-09-0002
Terminal Server Connections	-16-09-0003
Specifications & Functional Description	
Perfect place to store vendor specifications and manuals for network gear and other commercial equipment	-16-09-SNNN

System Engineering

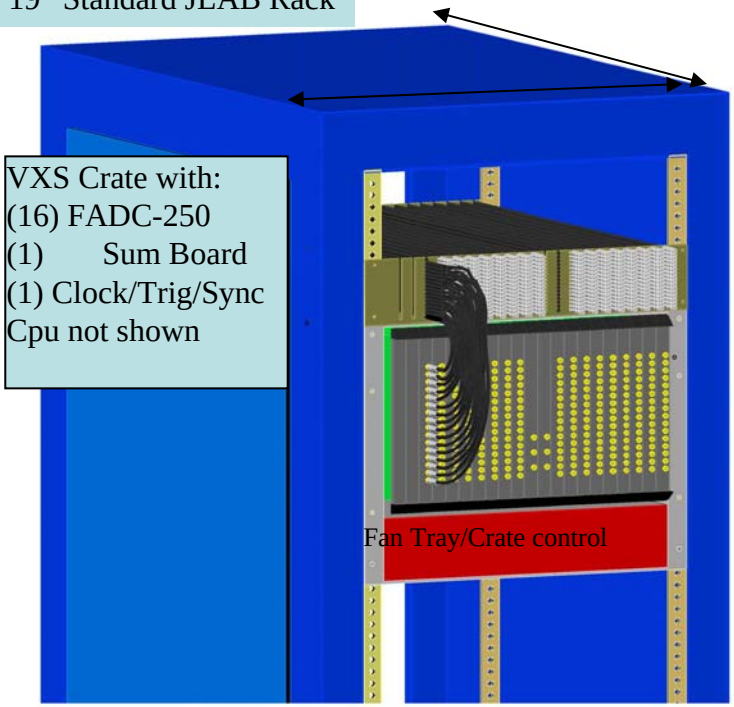
- Detailed system drawings are progressing nicely
  - These drawings are more than block diagrams
  - Details of every connection needed for a full functioning system
  - Specifications and model numbers for commercial equipment will be noted. (i.e. Fiber patch panels, cable types, connectors,,)
- Will need first draft ‘check’ before end of February
- Several specifications and functional description documents need to be created

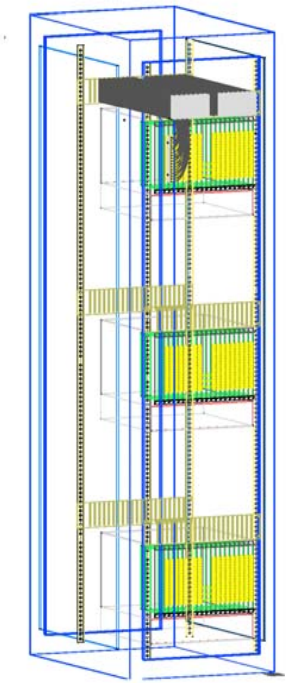
- After these system ‘logical’ drawings are complete we MUST begin the details of the ‘physical’ equipment rack layouts. (Analogous to schematic symbols (logical) to circuit board layout (physical)

- We will work closely with the Mechanical Engineers to capture crucial physical layout issues for each sub-system.

- Examples of physical rack layout drawings
- ALL equipment must be shown to identify rack space issues (i.e. Network gear, patch panels, splitter panels, etc.)
- Airflow/Cooling issues will need to be identified and resolved

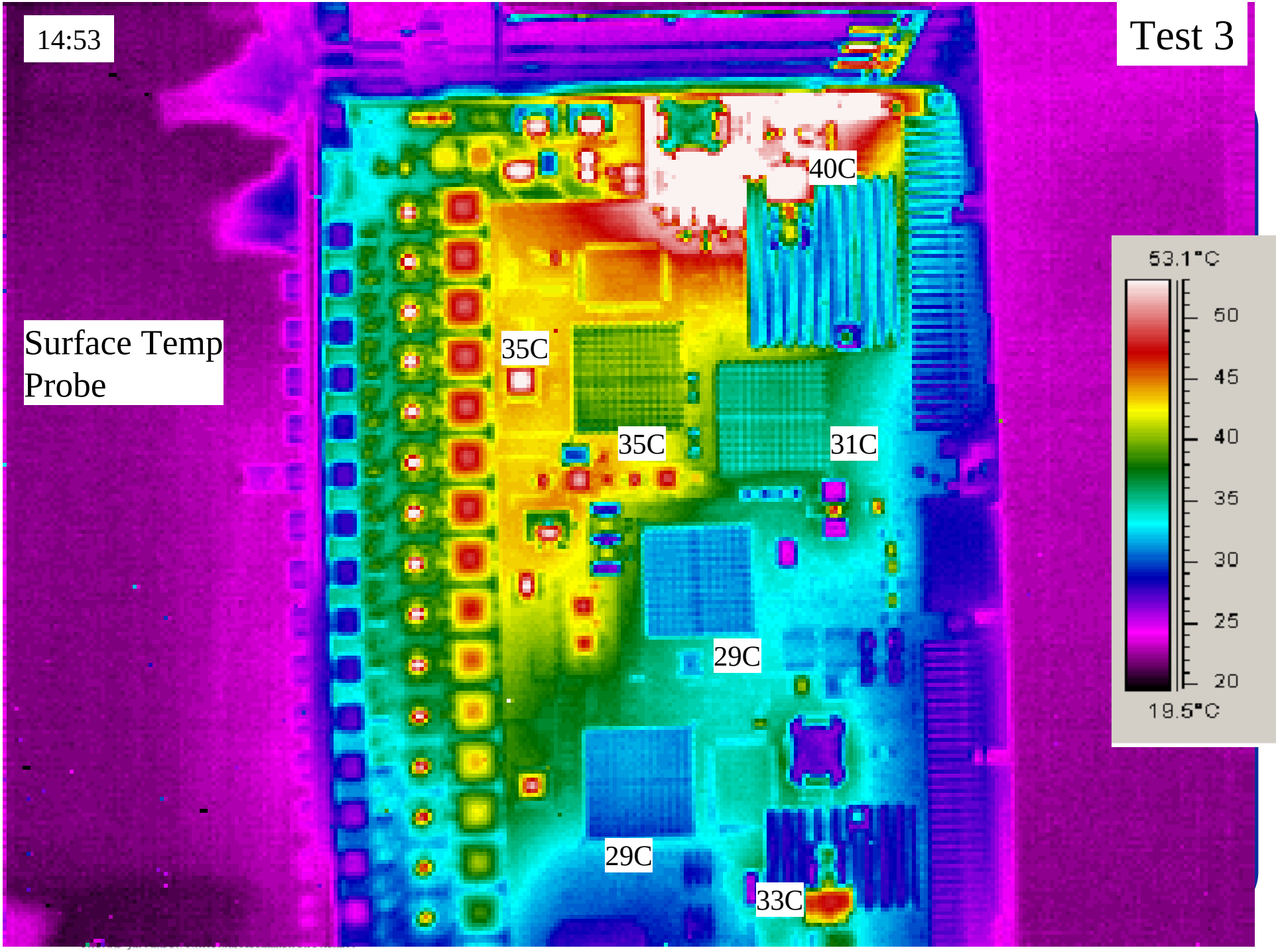
36” Deep
19” Standard JLAB Rack





Questions?
Discussion?

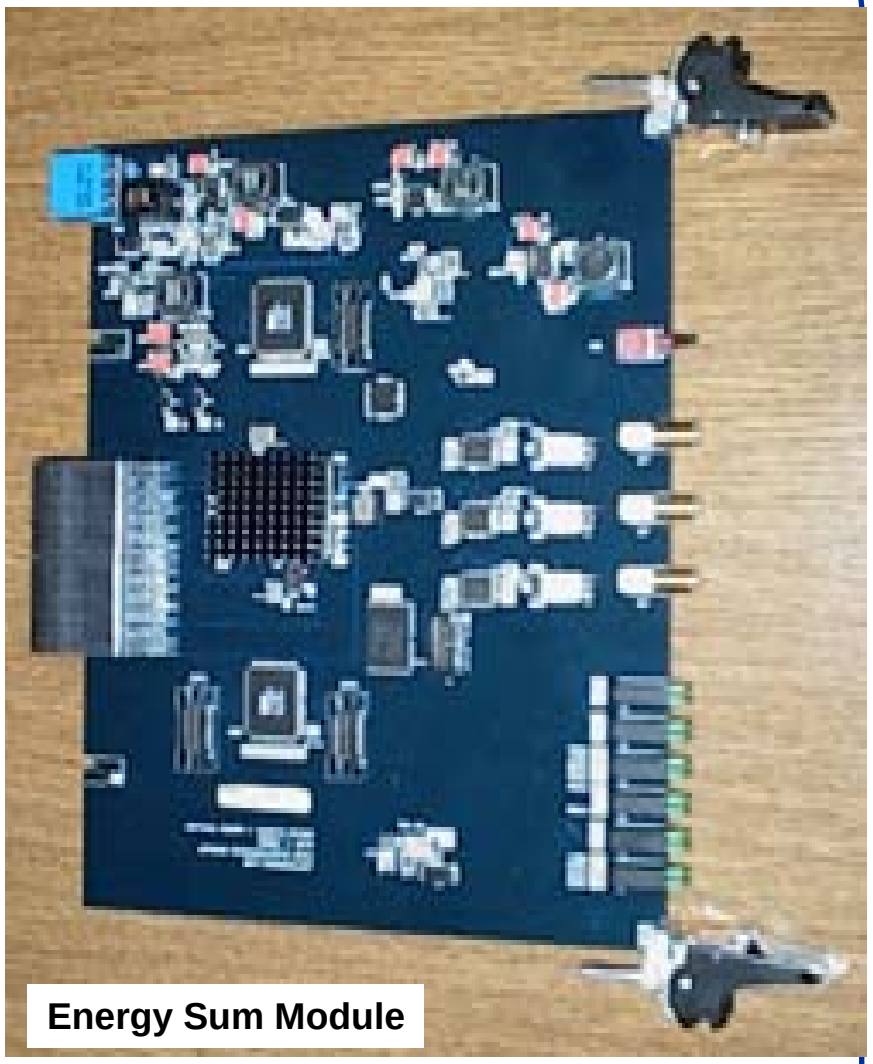
Other Stuff


14:53
Test 3
Surface Temp Probe
40C
35C
35C
31C
29C
29C
33C
53.1°C
50
45
40
35
30
25
20
19.5°C

Latest Designs

16 channel 250 Msps Flash ADC

VXS
High Speed
Serial
Backplane



Energy Sum Module