12GeV Trigger meeting notes:

8 Jan 20010: C. Cuevas, H. Dong, J. Gu, A. Somov, J. Wilson

18 Dec 2009: C. Cuevas, B. Raydo, H. Dong, J. Gu, E. Jastrzembski,

11 Dec 2009: C. Cuevas, B. Raydo, H. Dong, J. Gu, E. Jastrzembski, S. Somov, D. Abbott

November notes included

Updated prototype board status table:--8 January 2010

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** **SN001 ----------** **SN002 ----------** **SN003 ----------** **SN004 ----------** **SN005 ----------** **SN006 ----------** **SN007 ----------** **SN008 ----------**	 **Daq Lab F110** **Daq LabF110** **Daq Lab F110** **EEL – 126** **EEL109** **Hall C** **Hall A** **EEL – 126**	 **Test Board** **OK Hall A Student** **Moller Spare** **FDC test setup** **Needs repair** **Dave Mack & Steve Wood** **Moller setup** **FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded Sent to IU for FCAL testing 12Oct2009**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** Front Panel – Signal Distribution	**EEL109/DAQ Lab**	**Complete Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Testing complete**

0. Trigger/Clock/Sync – TI/TD

8 January 2010

Progress on the new TI/TD module was reported by William. The schematic work and initial component placement have started, and there will be details to resolve for the mechanical placement of a mezzanine board that will be used if a TI/TD board needs to be used in a legacy system.

William updated the status of the distribution module that will be needed for the Hall B CAEN 1290 TDC units. These TDC do not use VXS, so a distribution module has been specified and the design is progressing nicely. Up to 16 V1290 units will be connected to the distribution module. This distribution module will receive the clock, trigger, and synch signal from the TI via P2.

William, Ed and Chris met 'offline' to discuss the activity and preliminary schedule for the TI/TD project and Chris will generate a FastTrack schedule and add this project to the overall Trigger System schedule.

December 2009

We discussed the design concept for the production version of the trigger interface and trigger distribution module. William presented details of this design concept at the Hall D Online meeting and there was an enlightening discussion. Highlights of the discussion below:

- ➔ One circuit board design for TI and TD functions.
- ➔ Fiber transceivers will be populated depending on the TI board features that are required.
- ➔ Local subsystem crates can be connected together and one TI would operate as local TS
- ➔ Front panel I/O will occupy transceiver area, so initial assembly will determine what types of board features are available.
- ➔ Cost issues must be considered for TD and multiple transceiver versions of the TI. There are a limited number of subsystem configurations so the most cost effective TI version will only need 1 transceiver. Most of the sub-system crates will be in close proximity to each other, so expensive 12 fiber ribbon cable and transceivers may not be necessary.

At the Hall B collaboration meeting a new board requirement was declared for the Caen TDC. There will have to be a module that occupies a payload slot and distributes the required signals to the front panel of up to 16 Caen TDC. A simple specification sheet is needed and this module receives signals from the SD and P2.

- ➢ Decision for P2 I/O for the FADC250_V2 and F1TDC_V2 has been declared. There is NO need for P2 I/O connections because we have front panel distribution modules for Users that want a small number of modules for a lab test setup. If the Users need more modules in a test setup then they will use a full sized VXS crate and use the standard method to distribute the common signals to each payload board.

November 2009

Discussions regarding the new TI design and implementation plans have produced a number of good issues to solve. William has been working on the design files and there will be significant changes to the initial TI prototype modules. It may be a good idea to review the original specification documents and update this file with the new design requirements and added capabilities.

At the recent CLAS collaboration meeting, there was a good work session dedicated to DAQ and Trigger issues. Sergey showed the CLAS12 overall DAQ design which included the electronic modules designed for 12GeV trigger system requirements (CD-3; Hall D) The CLAS12 requirements are different than the other halls, and it was clear that there will have to be a module that will support the commercial TDCs that do not support VXS I/O for clock, trigger, and synchronization. All other modules in the 12GeV trigger 'family' will be implemented for CLAS12.

****** The Trigger Supervisor crate pair mapping diagram still needs to be created.

1. FIRMWARE TESTING

8 January 2010

No new firmware issues have been reported and Ed has been busy with converting the VME SST firmware from Altera 'HDL" to standard VHDL. This new VHDL version will need to be verified and will be used on virtually all new VXS payload modules.

There will be a number of firmware activities started once the SSP prototype module is assembled later this year, and William will also join in the development of firmware for the TI/TD units.

December 2009

All firmware issues have been resolved and tested by Ed and Hai. These firmware revisions have been uploaded to the specific FADC250 boards that are in use by several groups. See prototype board status table for board location details.

IU FCAL group is working with the timing algorithm. A few questions have been exchanged and they hopefully should have results soon.

November 2009

→An updated CODA library has been sent to the FCAL group at IU so that they can use the latest timing extraction feature on the 8 channel, 12bit FADC250 module. We are looking forward to the test results with the real FCAL PMT signals.

→The FADC250 unit used in Hall A for the Moeller application had a few issues that needed to be reviewed and resolved. Hai, Ed, and Dave A. have verified the changes and tested the upgraded firmware. The Hall experiment that will rely on this application is scheduled for March 2010. (PREx)

→The poster at the 2009 IEEE-NSS/MIC conference was presented by Jeff Wilson and he described discussions with a few participants that showed interest in the VME firmware transfer method. This method has been tested on a small scale and it would be worthwhile to test on several FADC250 in one crate. One of the problems is that the prototype modules are in use, so multiple board download testing will be delayed.

There are other implementation methods to download firmware 'bit' files to the front end FPGA, and most do not use the VME bus to transfer these files. Managing a transfer of new firmware bit files to the VME interface FPGA must be handled carefully because it would require a local download if the remote method failed.

2. *SUB-SYSTEM PROCESSOR (SSP)*

January 2010

The schematics for the SSP have been closely reviewed by Ben and Chris and the board placement activity is complete. This board is ready for routing and any long lead components should be purchased as soon as possible. The test plan for the SSP should also be drafted soon, and there are several trigger applications that have been proposed by the CLAS12 folks that will need to be reviewed before developing new firmware. The Hall D requirements for the SSP have been declared and reviewed, and give a firm starting point to test the performance of the SSP functions.

December 2009

The design of the SSP is ahead of schedule and the placement of the components on the payload board has been completed. Setting up the best board routing strategy will be the next activity and Ben has already performed functional simulation of the initial firmware. The transceiver protocol between CTP and SSP has been developed also.

The bill of materials has been reviewed to see if there is a way to consolidate the FPGA or other common components that will be used on other board prototypes. The BOM should also be reviewed and long lead items should be ordered soon.

Review of the schematics and functional descriptions/specifications/requirements has been requested. Chris (and others) will need to review these documents and check for consistency with other modules planned for the global trigger crate.

November 2009
Design progress is still ahead of schedule and Ben has been busy with another design that is at a higher priority so that production prototypes can be started.
→Given the board layout progress and preliminary firmware development, it would be a good time to update the specification document to include details about all the features. It is too early to describe a test plan using the existing CTP, but in principle the CTP could be used to provide test data to the SSP prototype and open up a whole new level of testing activities.

3. CUSTOMERS

8 January 2010
→VME64x mini crate and new GE Fanuc CPU have been shipped to IU. The FCAL group has been using the VXS crate that was loaned to Gerard and Gerard needs the crate to finish testing the FDC flash modules. There has been recent work and a few troubleshooting questions from the IU folks when using the latest 12 bit FADC250, and hopefully these issues will be resolved without having to send the unit back to Jlab for testing. Looking forward to the results from the timing extraction algorithm!
→The Hall C folks have not stopped by to pick up the test crate and FADC250 module yet. I will ask them one more time and then see what other group could use the module. I have a request from the Accelerator Injector group so we will see.
→No recent news from the Moller folks in Hall A. I believe they are on track to use the module for Prex coming up in March.

December 2009
Report that the IU FCAL group had sent a few questions regarding the latest timing extraction firmware that was updated in the 8 channel, 12bit version of the FADC250. Sounds like they are actively setting up to test the new timing algorithm and will be able to verify the results soon.
Hai and Ed have updated all firmware versions for the Moller application and the other flash boards have all been updated and tested.

November 2009
→See Section 1(Firmware) for details of the recent firmware iterations and solutions for the prototype trigger modules, including the FADC250. These firmware activities apply to requests/requirements from Users of the prototype units.

4 "B" Switch - Signal Distribution Module (SD)

8 January 2010
The SD module will need to be revised to reflect the changes to the signal pair mapping for the front end crates. We have two modules in the lab and I believe we can modify these units to work for testing the SSP prototype and revision 1 of the FADC250 that will be ready before the end of FY10. The SD module revisions are effectively only signal pair changes and there are a few other circuit changes that will also need to be included for the final production lot.

December 2009
No significant updates to report. Stay tuned as this module will need to be updated soon.

November 2009
→I have asked Abhishek to work on minor updates to the SD firmware so that he can continue with HDL development and testing. These firmware changes include the addition of counter registers to keep track of BUSY and Trig_Out from each of the payload modules. The TI reports the status of these signals at the crate level, and the SD can provide information for these

signals at the payload boar level. This activity is a lower priority, but test results will be forthcoming.
→No further actions on the SD design and the files have been imported from PCAD to Altium format. All changes (ECO) and any new required feature(s) will be revised with the Altium tool.

5. System Diagrams & Test Stand Activities

8 January 2010

This would be an appropriate place to note the discussion and ideas to test and commission the overall trigger system with simulation data that is loaded directly to the front end FPGA on the flash modules. The method to load these test data to the FPGA through VME has been developed, and there will need to be some software that can assemble and read the simulation data so that the front end channels are loaded properly for a given trigger system test.

Test patterns for a given sub system, would be loaded to the flash boards, and the SSP and GTP would be programmed to trigger if the given test pattern meets the trigger equation criteria. There are numerous possibilities here, and it was proposed to start with the development of software that would read and assemble data from a 'Physics' simulation, and process this data to the front end FPGA through VME. This development effort could start soon, and will certainly be essential once the trigger system is installed in the hall(s). Comments welcome and more discussions will follow.

December 2009

The front end VXS crate pair mapping diagram has been updated and this latest revision should be considered the final assignment. Collaborating institutions are requesting the pair map which includes signal level descriptions and pair polarity. The crate pair mapping is different from the original prototype design, and we have made these changes to accommodate the different modules for both the front end and global trigger crates and modules. For example, the TI module pair map is critical and has been finalized so that it accommodates the GTP modules that will reside in the global trigger crate. Other pairs from the SD to the payloads have been changed to accommodate new requirements for additional signals.

November 2009

Trigger test stand activities have been completed since May. New requirements and system layout proposals have been generated by Hall B (Sergey) for CLAS12. There have been other requests from a Hall A collaborator group for the specifications of the VXS pair mapping. This "12GeV VXS pair map" as it applies to the front end DAQ modules will need to be distributed to User groups that plan to deliver hardware (readout modules) for 12GeV experiments. One example is the SBS GEM application in Hall A, and I am sure there will be others that will design modules on the VXS format.

Crate Trigger Processor (CTP)

10 July 2009

CTP activities are complete.

6. Projects for FY10

8 January 2010

→Project schedule updates have been reported to the project management team. It has been noted that funding for procurements in the BIA activities are missing, so allocating funding for the purchase of prototypes for SSP, TI/TD etc will have to be extracted from 12GeV funding or a combination with 6GeV operations accounts.

December 2009 Projects are still progressing well and on track. Review schedule in Jan 2010.

November 2009

Projects defined for FY10 are on track and progressing well. Several key decisions have been made for these projects and I do not see any major obstacles to meeting the goals planned for FY10.

ACTION ITEMS: **Next meeting → Friday 15 JANUARY 2010 at 11:00am in F228**

HAPPY NEW YEAR!