12GeV Trigger meeting notes:

1-June-2012: C. Cuevas, W. Gu. H. Dong. B. Moffit, S. Kaneta, B. Raydo, N. Nganga, E. Jastrzembski

18-May-2012: C. Cuevas, W. Gu. H. Dong. B. Moffit, S. Kaneta, B. Raydo, N. Nganga, A. Somov, E. Jastrzembski

11-May-2012: C. Cuevas, W. Gu. H. Dong. J. Wilson, B. Moffit, S. Kaneta, B. Raydo, N. Nganga, A. Somov

4-May-2012: C. Cuevas, W. Gu., B. Raydo, H. Dong. S. Kaneta, N. Nganga, E. Jastrzembski

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0. Trigger/Clock/Sync – TI/TD

1-June-2012

→TI-D contract has been awarded to CEM on 29-May-2012. 22-August is the date for 15 1st article assemblies. A vendor QA visit before production begins has been proposed, but no travel plans have been confirmed...
→Sergey has returned the TI and SD boards from the Hall B HPS setup. Cody Dickover will receive at least one of the pre-production SD boards to test the FADC125. Hall D already has at least four TI boards, so William would like to know why they need another board for Cody.
→There were operational issues during the HPS run, that have not been resolved. A total of 3 crates were used during the HPS run and there were several issues. Sergey has the error list and these errors should be understood and resolved.
→Global Trigger Testing – Some discussion on what the testing includes.

- GTP→TS: Verify four DensiShield ports/cables
- Use SD and SSP (and FADC250?)
- Trigger Distribution → TS→SD→TD(1); TD(2)→TI(1);TI(2)

18-May-2012

→We will begin to setup the global trigger crate testing with TS and GTP in the EEL109 lab by the last week in May. We will need to wait until we collect the FADC250 boards from Hall B beam setups.
→Cody D. will need SD and TI for initial testing of the FADC125 VXS I/O. SD and TI boards *should* be available in a week or two.
→No new news on the contract award, but William has been in contact with Kathleen and there are plans for a QA visit one of the qualified vendors.
→We had a good discussion on trigger signal parameters and the need for a simple table that outlines these parameters (per front end DAq board) is evident. Any volunteers? Maybe these parameter values are spelled out in the manuals for the front end DAq boards?

11- May-2012

The TI-TD production contract has not been awarded yet, and this procurement has been in the queue for 5 months! There have been a number of funding issues, but the Technical Evaluation Team summary is COMPLETE!

TS functional testing is completed and ready to install in a full global crate test setting.

→There has been a few emails and discussions regarding the MIN-MAX parameters for the Trigger signal output width, signal separation, signal duration, number of signals for a given time duration, etc. I think that we should create a simple table that includes a Trigger I/O parameter definition and lists the MIN-MAX values for each particular front end board. For instance:
FADC250:

MIN Trigger1 signal pulse width (MAX?; Default?)
MIN Trigger1 signal separation (MAX?)
MAX number of Trigger1 signals within Ntime
The table should include all signal parameters for I

4 May 2012
The final award for the TI-TD boards is almost 'official' and the TET summary report has been submitted to procurement.

William has started to draft a TI-TD acceptance test procedure and the procedure should be used by another person to provide feedback.

William continues to test the TS first article board and so far the testing is progressing.

At some point in the next few weeks, we should install TS, SD, GTP, SSP and as many FADC250 boards to begin Global Trigger Crate integration testing. 6GeV beam will stop on 18-May, so in principle we should have at least enough FADC250 boards for a full crate test. The FADC250 boards in this case would serve as data generators to the GTP.

1. *SUB-SYSTEM PROCESSOR (SSP)*

1 June 2012
→Schematics and ECOs have started. Ben would like to begin specification and procurement cycle as early as reasonable and will need the final BOM and fabrication details. The quantities have been known for some time.

18-May-2012
→Start 1 June on ECO and procurement for at least the Hall D quantities.
→After a brief discussion, Ben will consider the cost/performance gain by using the best versions of the Xilinx V5 parts. (Speed grade, etc)
→Very good results from the latest HPS test run in Hall B. The SSP performed well with two crates and processed cluster triggering from the two CTP.

11 May 2012
Will resume production project updates in late June 2012. No issue at all for the HPS test run.

4 May 2012
SSP is successfully installed and used in the HPS global trigger function. The SSP is presently collecting trigger data from two crates to form final quadrant cluster triggers.

2. *CUSTOMERS*

1-June-2012 →PePPO
Positrons are being produced!!
Only a few reports of questions etc., but they are collecting data consistently.
Trigger optimization has been worked on by Bryan, but significant issues have been eliminated.
→The FADC250 TDC function has been re-tested and understood. It appears that certain input signal shapes will cause problems with the TDC value that is reported. Firmware that captures the peak value will be modified. Hai started a discussion about TDC + Integral as one mode and this firmware revision will require documentation and requirements.

18-May-2012
→**PEPPo** tour anybody? So far all 'customers' are rather happy and the work efforts are impressive. The PEPPo experiment will run until the end of June.

→Was the FADC250 TDC function resolved? The topic was discussed at the GlueX collaboration meeting, and from my understanding, it seems they were operating in a mode where the TDC function was not reporting the TDC value correctly.

11-May 2012
-->13th FADC250 was borrowed from DAq lab and now installed in the 2nd crate of the HPS calorimeter detector in Hall B. The DAq is a symmetrical setup now, and Scott has been working on latest change request for the CTP firmware. These new firmware changes if completed, will hopefully be loaded to the CTP before the beam test period on Friday 18-May.
→FCAL test in hall B would like to implement the TDC function. Appears to be a problem with the existing firmware, and Alex would like this to be investigated. There is only 7 days remaining of beam test, so there is some hope of using the TDC feature.

4-May-2012
→HPS installation went well, and initial results look promising. Calibration of the detector components etc are in progress. Experiment plans not clear, but only a few weeks of beam remain for the test.
→PEPPo group is ready for experiment and custom firmware is complete for their boards.

3. *"B" Switch - Signal Distribution Module (SD)*

1-June-2012
-->Start the new and improved SD acceptance test procedure with as many FADC250 pre-production boards as possible.
→Notes about pre-production board locations has been posted to the wiki

18-May-2012
→New and improved acceptance test procedure is ready for an initial run! The idea is to use up to 16 FADC250 to fully test the SD I/O and other critical functions.
→Production contract is moving along without any significant issues. On track to receive 10 1st article boards by June 20th, 2012.

11-May-2012
→The final production manufacturing files have been shipped to CEM.
→Nick has re-written the SD acceptance test procedure and in a few weeks we will have at least a crate's worth of the pre-production FADC250 boards back in the EEL109 to proceed with a test of the test procedure.

4 May 2012

→Production fabrication and assembler award is official: Subcontract JSA-12-C1484
The company that won the award is CEM.
The production front panels have been received.
Final manufacturing files have been delivered to procurement for distribution to CEM.
→Acceptance test procedure is a work in progress and will need to be revealed soon. We will need to have at least 16 FADC250 boards to proceed with the production SD acceptance test.

4. *System Diagrams/Fiber Optics*

1-June-2012
→Chris will proceed with an order for the fiber optic patch chassis and panels for the halls. There is no reason not to proceed with this part of the order. The patch cables and trunk fiber will be ordered together and the fiber specification still needs to be finalized.

11-May-2012
→Brad S. has provided fiber lengths for the required MTP cables that will be used both the HMS and SHMS spectrometers. The number of MTP connections are low, so I suggest using trunk cables that only have 2 twelve fiber ribbons.
→After the 6GeV beam is turned off, and the test (patch) cables are surveyed from the Hall, we can run a quick test to see if the MTP cables were damaged.
16 March 2012
Brad S. (Hall C) suggested a simple MTP Fiber test in hall c using a few of the short jumper cables. The suggestion is to simply place a fiber patch cable in Hall C for the remainder of the 6GeV experiment and then test the fiber cable to see if there is any transmission problem. Setting up an 'active' test would take some effort with hardware/software using an evaluation board and the 150m fiber. This way a measurement of fiber degradation over a finite time interval with a known dose rate could be achieved. Ben, Chris, Brad.

5. Two Crate DAq test configuration

1-June-2012
No specific update, but the ROC procurement for the production quantities is progressing. It is not clear if the production units will be delivered in coincidence with the delivery of the FADC250 boards, but that is not a critical issue. The full crates can be tested regardless of the ROC delivery.

18-May-2012
→Bryan presented his work on the procedure outline for the full crate test station. The tested FADC250 boards will begin arriving from UMass in about a month, so we will have to dedicate an existing CTP, SD, and ROC to fully verify 16 FADC in a crate. This test will verify that all FADC250 in a crate function properly in unison with the trigger boards, and the populated crates can be relocated to the respective Hall (or storage).

11-May-2012
→Plans to begin testing the 'global crate' will become reality as soon as we can assemble one VXS crate in the EEL109 with TS, TD, SD and GTP. The SSP in principle, could be used but it may make more sense to use a few FADC250 boards to generate "L1 Trigger Data" to the GTP. There are many test parameters that need to be measured, recorded and verified.

4-May-2012
→We do not have to rely on two VXS crates for future testing, and the next goal is to complete a procedure for a semi-automated test using 16 FADC250 with the full suite of TI, SD, and CTP boards. I believe the CODA libraries and board firmware are at stable versions, so software and a few GUIs are next.

20-JAN-2012 (Keep this date reference full DAq crate procedure)

3 June 2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!

16 July 2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

6. Crate Trigger Processor (CTP)

1-June-2012
→Schematics are complete
→Finalize lane assignments from PP17 (The ROC)

→Final version of CTP will have FPGA remote programmability via:
TI (I^2C)
PP17 (Option)
→The procurement cycle can begin once we finalize the latest BOM, layer stack and preliminary fabrication drawings. A draft CTP specification has been generated and will be updated soon so that we can begin the approval process and funding allocations.

18-May-2012
→Need to get the schedule updated.
→Schematic translation work still in progress
→Plan to start procurement PR in the system so that we can do our best to order these by end of fy12.
→Nick has volunteered to be the Altium database library manager.
→ECOs are well documented and added features are finite.

11-May-2012
→Need to review the schedule. Schematic will be ready in three weeks. BOM, etc can be used for cost estimates and 'bids'.
→Procurement (FY12) will include the Hall D quantity only.
→Review the implementation of the "PP17" and include the Gigabit connections from the ROC slot.(PP17) to the CTP FPGA. The single board procurement has started, so the source selection will determine what 'protocol' is specified for the VXS connection.

4 May 2012
→Hai reports that the schematic is progressing and decision to use FXT series has been priced and selected for the Hall D quantities. Goal for production orders remains and these boards need to be ordered before end of FY12!
→UDP Ethernet 'soft core' has been tested and will be tested on the GTP.

7. GTP and Global Crate Developments

1-June-2012
→VXS Aurora transceiver code to implement (SSP) data transfer.
→Borrow transceiver from CTP or SSP to test fiber transceiver section
→Prepare for GTP→TS testing
→Ethernet development is progressing

18-May-2012
→Ethernet hardware is running on the GTP. MAC supports the PHY that Scott implemented on the Altera part.
→Fiber Transceiver still needs to be tested. Scott will use FADC250 boards as pseudo-SSP data generators. It would be a good opportunity to include 5Gb/s testing as well.

11-May-2012
→Ethernet code transferred to Scott from Hai. Simulation is progressing.
→Setup in EEL for global crate testing.

4 May 2012
→ The GTP to TS high speed output link will need to be tested in a VXS crate including the TS rear transition card. Ethernet implementation has been started and Scott has a copy of the Ethernet source code for further development and testing. The fiber optic transceiver section still needs to be functionally tested before considering this option for the production boards.

***ACTION ITEMS*: Next meeting -Friday 8 June @ 10AM in F226**