Trigger/Clock Distribution Prototype Status

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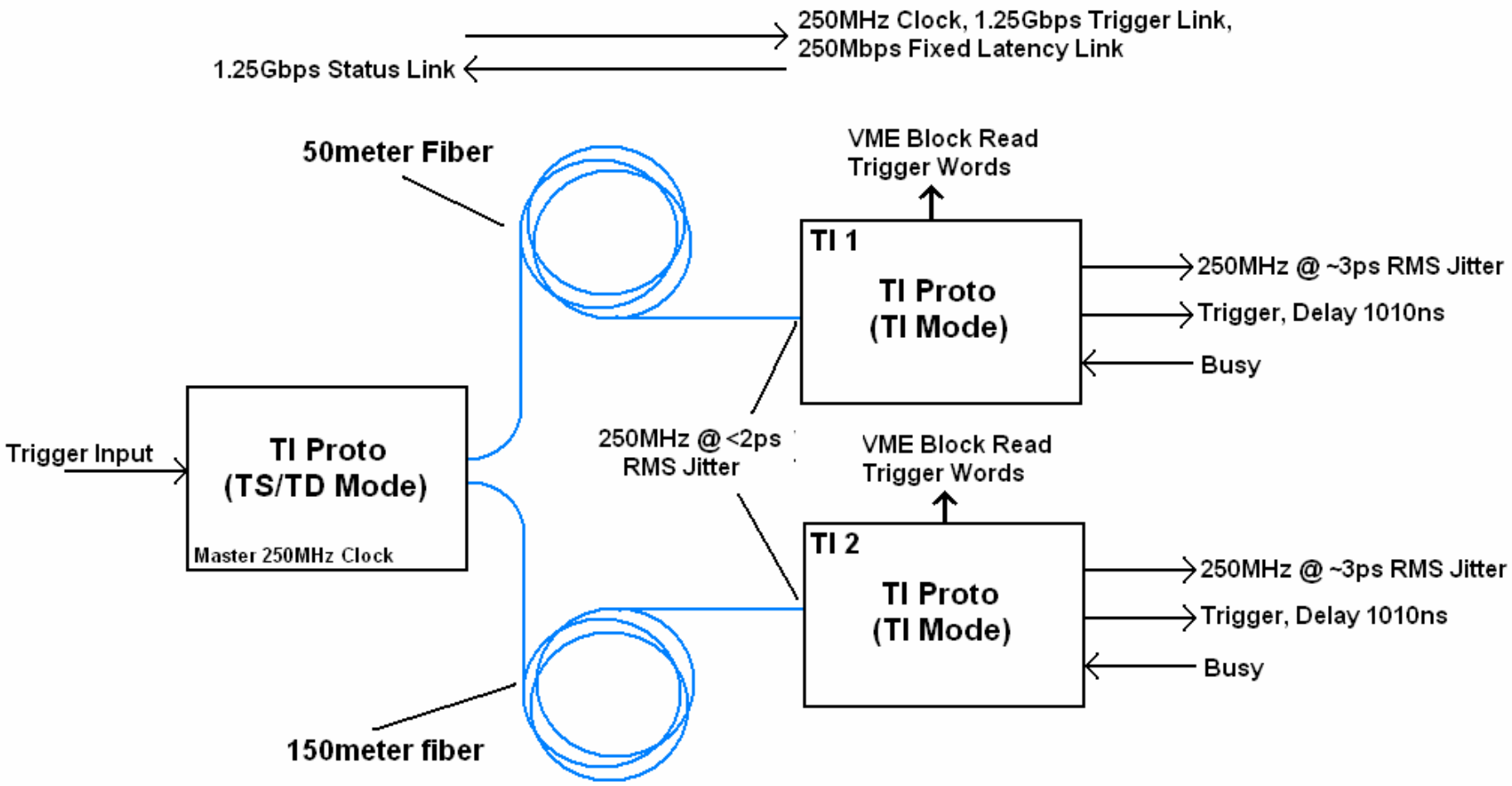
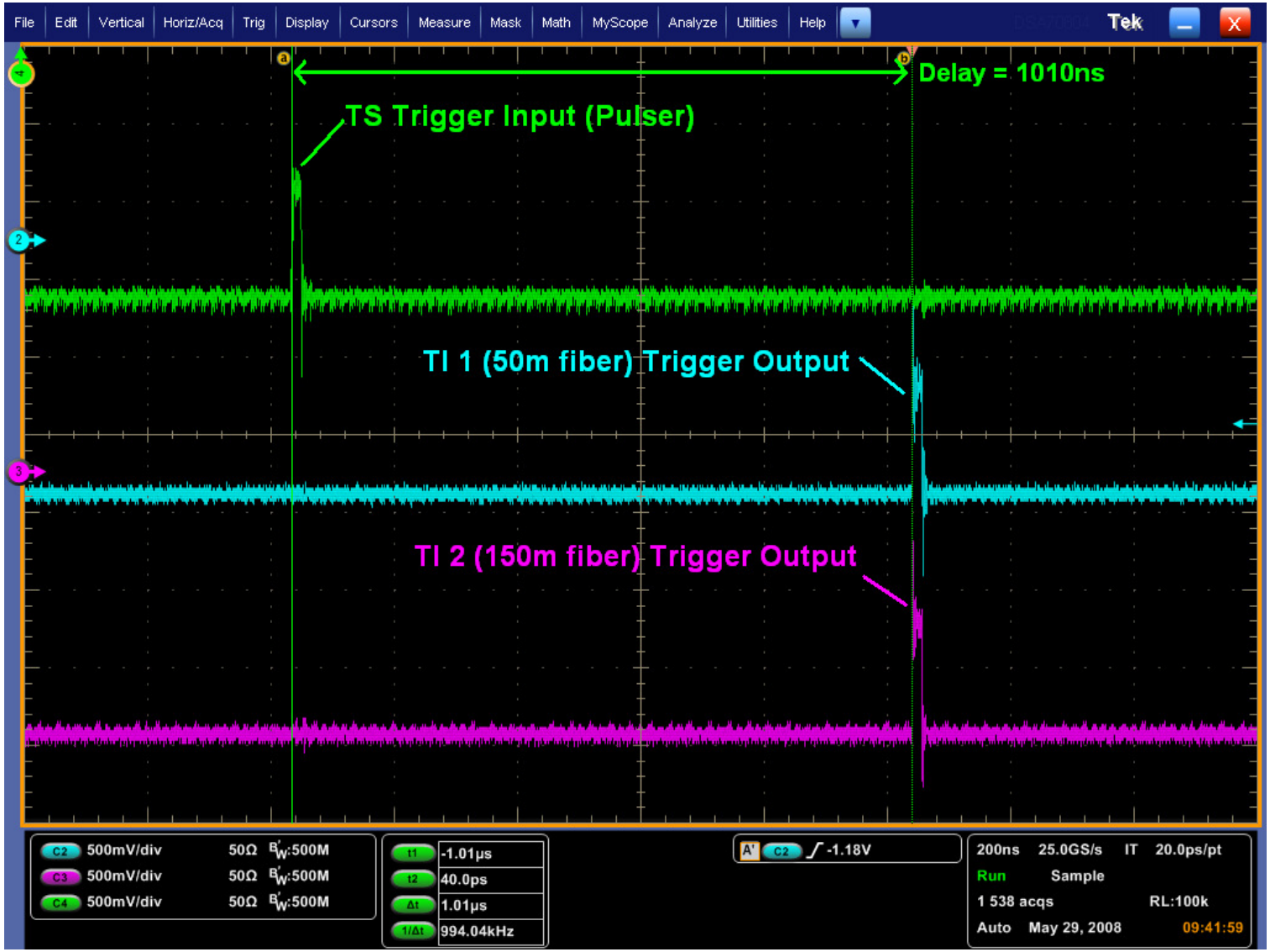
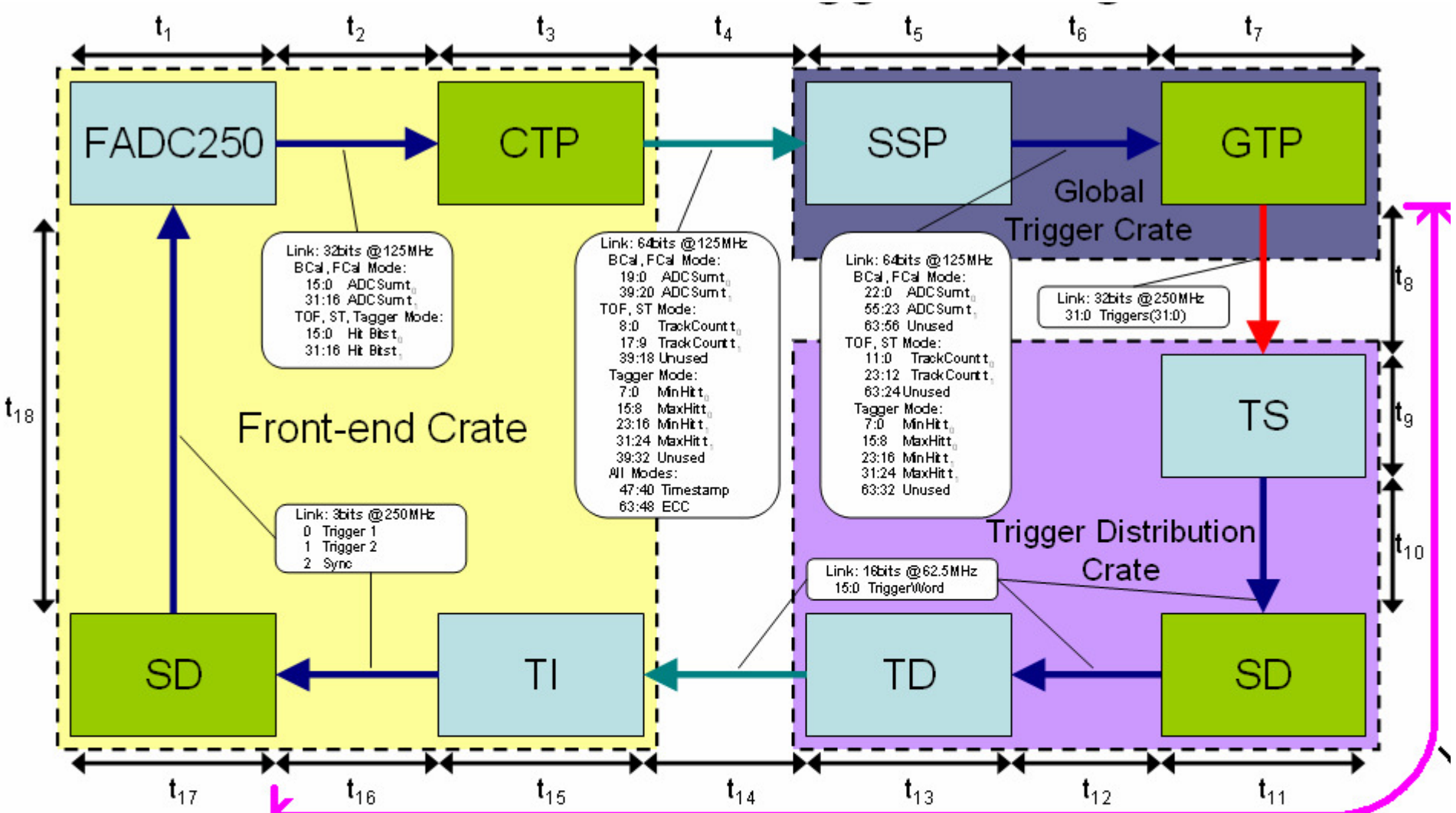
Test Setup


250MHz Clock, 1.25Gbps Trigger Link,
250Mbps Fixed Latency Link
1.25Gbps Status Link
50meter Fiber
VME Block Read
Trigger Words
TI 1
TI Proto
(TI Mode)
250MHz @ ~3ps RMS Jitter
Trigger, Delay 1010ns
Busy
Trigger Input
TI Proto
(TS/TD Mode)
Master 250MHz Clock
250MHz @ <2ps
RMS Jitter
VME Block Read
Trigger Words
TI 2
TI Proto
(TI Mode)
250MHz @ ~3ps RMS Jitter
Trigger, Delay 1010ns
Busy
150meter fiber

Trigger Distribution Delay



Triggers Arrive Simultaneously on Different Crates with Different Length Fiber Cable



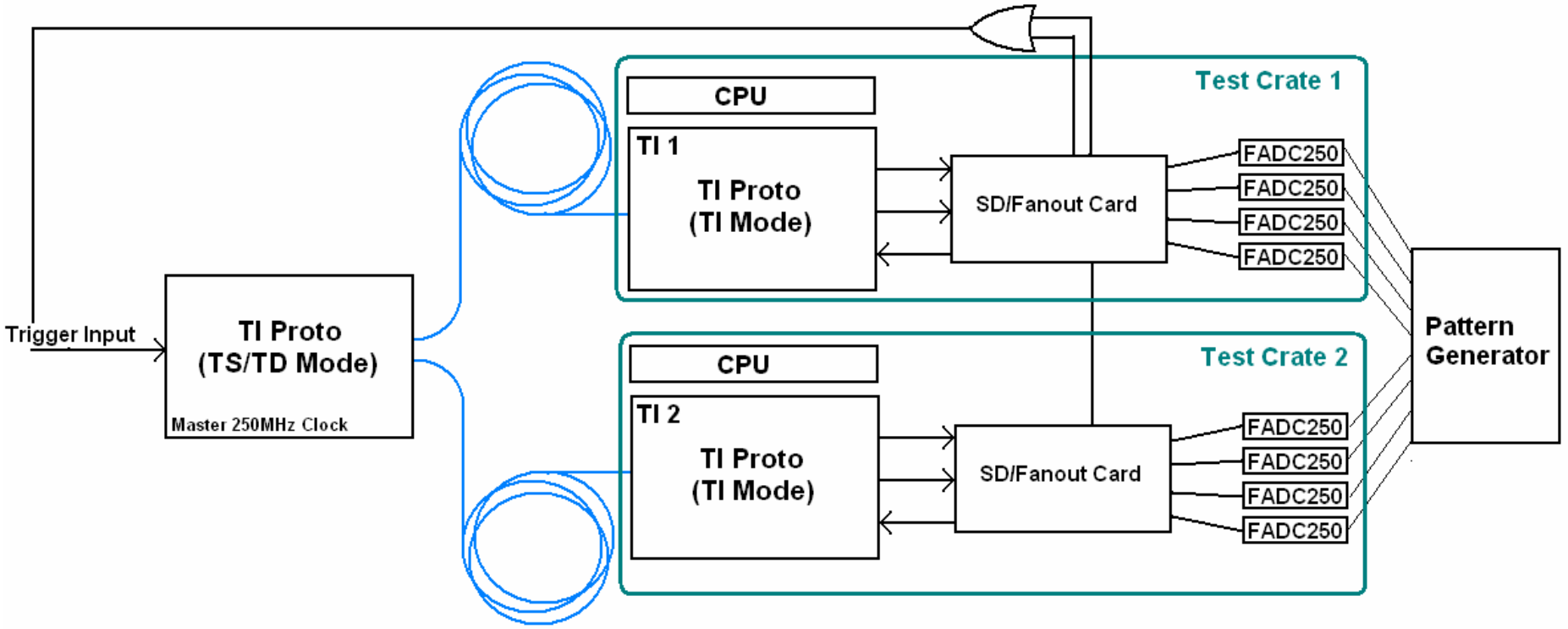
t_1: FADC250 (ADC->P0)	180ns (20cycles+100ns MGT)	t_{11}: SD (Px->Px)	10ns
t_2: FADC250->CTP (P0->Px)	10ns	t_{12}: SD->TD (Px->P0)	10ns
t_3: CTP (Px->FiberTx)	180ns (20cycles+100ns GTP)	t_{13}: TD (P0->FiberTx)	10ns
t_4: CTP FiberTx->SSP FiberRx	600ns (~100m fiber run)	t_{14}: TD->TI (FiberTx->Fiber Rx)	600ns (~100m fiber run)
t_5: SSP (FiberRx->P0)	600ns (100cycles+200ns GTP)	t_{15}: TI (FiberRx->P0)	80ns (20cycles)
t_6: SSP->GTP (P0->Px)	10ns	t_{16}: TI->SD (P0->Px)	10ns
t_7: GTP (Px->TrigBit)	495ns (95cycles+100ns GTP)	t_{17}: SD (Px->Px)	40ns
t_8: GTP->TS (TrigBit->TrigBitIn)	10ns	t_{18}: SD->FADC250 (Px->P0)	10ns
t_9: TS (TriggerBitIn->P0)	115ns (20cycles+35ns SerDes)	t_{19}(?): FADC Buffer Processing	0ns (?)
t_{10}: TS->SD (P0->Px)	10ns		
Total:	**2980ns**		

Fiber Optic Lin
Copper Ribbor
VXS Backplane

Trigger Latency Adjustment

- Trigger/Clock Distribution Prototype acheives 1010ns latency with maximum 150meter length fiber
- 3µs Trigger Timing Diagram assumes maximum 100meter length fiber in trigger system (to Tagger)
- Adjusting for ~250ns added latency from the extra 50meter fiber puts the Trigger Distribution Latency at ~760ns (~100ns faster than Trigger Timing estimate)

TI Proto in Test Stand Setup



1.25Gbps Trigger Link