THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY
12000 Jefferson Avenue

HALL D PROCEDURE NO.:
D00000-04-02-P002 Rev C
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TITLE: Hall D Solenoid Commissioning DATE: 2/4/2013

BY: Joshua Ballard

CHK: George Biallas

APP: George Biallas

APP: Timothy Whitlatch

REV.	DESCRIPTION	BY	CHK.	APP.	APP.	DATE
C	Extensive revision to follow on to Rev. B. Verify remaining interlocks, commission PLC Quench Detectors, Soft ramp to 140 A and back to zero.					
B	Extensive revision to include Power Supply Qualification at 15 A, the interlock verification necessary, verification of Ground Fault Detector placement, test for turn-to-turn shorts, calibration of the Quench Detector and leaving final cool-down to LHe temp.					
A	Incorporated changes recommended by reviews. Updated to reflect actual installation	JTB	TW for GB	TW for GB	TW	2/22/13

Re - Commissioning Goals – Intermediate (140A) Current

1. Re-verify correct operation of remaining mechanical, cryo, safety and control/monitoring/archiving systems not addressed in Revision B
2. Demonstrate that the Solenoid remains a viable Superconducting Magnet up to this current limit for portions of an hour.
3. Verify that the Ground Fault Detector doesn't trip the interlock string over this current range
4. Verify that the Magnet Power Supply (MPS) is capable of starting and stopping ramps to more than 15 A, using the soft ramp without tripping the Quench Detectors (QD).
5. Provide a greater ramping range over which the balance, sensitivity and offset of the Quench Detector can be verified and adjusted
6. Demonstrate stable cryogenic operation with a full LHe vessel.
   Demonstrate soft ramp profile ramp-down to 0A without tripping the QD.

Administrative Requirements

Perform all Solenoid Operations per the Operational Safety Procedure (OSP)

Perform the remaining items in D000000402P007RevASolenoid Pre-Power Up Checklist associated with cryogenics and vacuum.

It is assumed that Revision B of this Commissioning Procedure was performed and that interlock verifications made under that Revision are still viable (If the circuitry was modified in the interim revisit those interlock tests)

The Solenoid shall be full of Liquid Helium per the latter part of Revision B of this Procedure in order to start Revision C.

Final Vacuum System Checks

1. For all non-pumped coil-insulating volumes, is the key switch in "Closed" position and the key removed to the Key Safe?
2. For all pumped coil insulating volumes, (1) is the Turbo Pump up to 1000 Hz speed, (2) is the key switch in "Automatic" position and the key removed to the Key Safe?
3. Are pump-out valves on the Roots Valves at the Chimney, on the chimney vacuum gages and on the Side Port vacuum gauges administratively locked out?

Hardware Fast Dump Interlock Verifications

The following hardware fast dump tests verify that hard-wired interlock systems, not tested under Revision B, operate as expected.

If the SOE System is repaired and operational for this test, verify that the SOE indicates the appropriate "first-fault" at every interlock test below. If SOE indicates incorrectly, note the circumstances in the Elog for the item and continue to the next item.

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IMPORTANT!

Continuously monitor voltage taps during fast dumps for excessive voltages. Large voltage spikes (> 5 V) that occur during a fast dump may be an indication of an open dump circuit. If voltage spikes occur, halt testing immediately, determine cause of voltage spikes and mitigate as appropriate.

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1. Voltage tap circuits, quench protection circuits, pick-up coils, PXi system and archiving system shall be operational. Turn on the PLC archive and PXi System, initiating a recording session named by the date and time.
2. Zero the PXi data logging system.
3. Remove all "Buggers" in the system or be aware of necessary buggers and log that the operator accepts them. Consult the ABIL System for Hall D under "Useful Links " on the JLAB Logbook page.
4. Set MPS front panel ("CEBAF") overcurrent set point to 20 A. Set Newport overcurrent detector set point to 15 A. Set PLC overcurrent limit to 15 A. Set slew (ramp) rate to the successful ramp "after start" rate achieved in the last commissioning plan.
5. Turn on the MPS. Reset so the Dump Contactor closes. **The** requested current shall be zero. Verify supply is turned on.
6. Observe if the transients still trip the QD upon Power Supply's turn-on.
7. If the QD trips, dis-engage the QD using the momentary switch and turn on the MPS again. Re-engage the QD by letting go of the switch. Use this method to turn on the Power Supply if required for all future actions of this procedure.

VCL FLOW CONTROLLERS – Fast Dump

8. Disable PLC VCL Flow interlock by setting VCL Interlock threshold to 0.0 SLPM.

9. Halt flow in upstream VCL mass flow controller by closing the associated valve. Verify initiation of fast dump by hearing Dump Contactor open. Verify SOE "VCL Flow" (if operational). Restore lead flow and turn power supply back on. Reset the MPS.
   Halt flow to downstream VCL mass flow controller. Verify initiation of fast dump. Verify SOE "VCL Flow" (if operational). Restore lead flow and re-enable PLC VCL interlock by setting VCL Interlock threshold to 2 SLPM.

QUENCH DETECTORS – Fast Dump

10. Set the balance setting on all QD and PLC QDs to match the ratio of the inductances at zero current in elog **3154577**. Disable the PLC Coil Quench Detector and the PLC Tap-Coil Quench Detector by setting their voltage thresholds to 10 V.
11. Reset the MPS. With all quench detector switches on the Test Box open (Toggle Down) and the QD's fast dump string circuit defeated by shorting leads, simulate a quench using Voltage Tap Test Box on Channel 1's Coil Sets and verify tripping around the 100 mV threshold. Verify initiation of fast dump. Verify SOE "Quench Detector" (if operational)
12. Repeat Step 12 for the remaining two channels of the hardware quench detector. Verify SOE "Quench Detector" (if operational).

Note 14 through 18 may be performed as part of the Pre-Power Up Checklist. The solenoid need not be at LHe temperature or the MPS connected to the Solenoid.

13. Keep Test Box QD (only) switches open and the QD fast dump string circuit defeated. Re-enable all Channels of the Tap Coil Quench detectors by setting the software trip value to 100 mV. The MPS does not have to be on for the following, Trip is indicated by indication of tripping of the PLC Fast Dump Chain.
14. Introduce voltage (using a voltage source) to the individual PXi Channel associated with each internal lead and Tap Coil to establish its actual trip voltage. Accomplish this by un landing the individual pairs of upmost leads, coming from the coils, on the upper terminal strip (TS-IDB310-1) in the Voltage Tap Distribution Box (D000001613-0310). Introduce increasing (absolute value) positive and then negative voltages on each voltage tap pair until tripping the PLC Tap Coil QD. Record the value in the table attached in Appendix 1.
15. The first PLC trip of item 16 verifies the PLC Fast Dump Relay. The SOE should indicate "PLC Fast Dump" (if operational).
16. While at each un-landed position, disable the Tap Coil QD by raising its threshold to 10 V and enable Channel 1 of the PLC Coil QD by lowering its threshold to 100 mV. Introduce voltages to verify tripping at the threshold value. Adjust the trip points such that threshold for all trips remain less than 105 mV. Record the readings in the above table. Re-land the leads to their original terminal position.

17. Repeat item 17 for enabled Channel 2 and then enabled Channel 3 (disabling other channels) of the Coil QD. Continue through the 21 pairs.
18. Re-enable all PLC QD Channels by setting their threshold to 100 mV. and close (raise up the toggle) of all the Test Box Switches and remove the shorting leads from the QD Fast Dump chain. The re-landing in the correct positions of all wires above shall now be verified by an independent person re-checking the wire re-landing. (If the option of performing the above during Pre-Power Up Checklist, while above LHe temp, the small power supply may be used at up to 10 A through the solenoid and the individual Tap-Coil voltages may be read by the PXi to verify proper wire re-landing. The main MPS leads may be attached to the Solenoid but the MPS Breaker must Lock & Tagged out)

LOWER VCL OVER TEMPERATURE – Fast Dump

19. Turn on the MPS and reset. Simulate VCL cold end over temperature by adjusting the relay set point for LakeShore #2, Channel #1 to 3 K. Verify initiation of fast dump. Verify SOE "VCL Over temperature" (if operational). Reset relay set point to 8 K. and reset the MPS
20. Repeat Step 19 for LakeShore #2, Channel #'s 2, 3 and 4.

VACUUM CONTROLLER – Fast Dump

21. Test Coil 1 vacuum interlock by adjusting the relay set point for Coil 1's Cold Cathode vacuum controller to a value BETTER than the current vacuum pressure in Coil 1. Verify initiation of fast dump. Verify SOE "Vacuum Failure"(if operational). Reset relay set point to $1x10^{-5}$ Torr. Reset the MPS.
22. Repeat Step for the remaining 3 coil and distribution box vacuum controllers.

PLC Fast Dump Interlock Verification

The following steps test the PLC Fast dump items. For each test, verify that the SOE indicates the proper "first-fault" (PLC Fast Dump, in this case) (if operational).

1. Reset the MPS. Set PLC Helium Pressure Fast Dump limit to 0.9 Atm Absolute. Verify initiation of fast dump. Reset PLC Helium Pressure Fast Dump Interlock limit to 2.1 Atm Absolute
2. Reset the MPS. Set PLC vacuum limit to <1e-10 Torr on each of the 5 Cold Cathode Gauge readings. Verify initiation of fast dump for each. Reset PLC Interlocks to <1e-5 Torr.
3. Reset the MPS. Set PLC Helium Differential Pressure limit to 100%. Verify initiation of PLC Fast dump. Reset PLC helium Liquid Level to 35%

PLC Slow Dump Interlock Verification

The HMI MPS and Interlock screens should indicate which interlock tripped in tests below.

Use a Flagged "Test Jumper" to defeat the hard wire interlock corresponding to any respective software interlock.

PLC OVER CURRENT – Slow Dump

1. (Perform this check only if Local Mode is available) Set PLC overcurrent set point to 10 A. Turn on the MPS and reset. Switch Power Supply to Local Mode. Attempt to ramp to 15 A. using the Knob control. Verify initiation of slow dump as current passes 10 A. Reset overcurrent set point to 145 A and reset MPS to Remote Control.

VCL LOW FLOW – Slow Dump

2. Insert hard wire jumper in Upstream VLC interlock. Turn on the MPS and reset. Halt Upstream VCL flow. Verify initiation of slow dump. Reestablish flow through Upstream VCL. Remove jumper.
3. Insert hard wire jumper in Downstream VLC interlock. Reset the MPS. Halt Downstream VCL flow. Verify initiation of slow dump. Reestablish flow through Downstream VCL. Remove jumper.

HELIUM HIGH PRESSURE INTERLOCK – Slow Dump

4. Reset the MPS. Set PLC Helium Pressure Slow Dump High interlock limit to 0.9 atm. Verify initiation of slow dump. Reset PLC Helium Pressure Slow Dump High Interlock to 1.4 atm –

HEIM COLUMN STRAINS – Slow Dump

5. Reset the MPS. Set PLC Axial Column Force limit to 0.1 lbf. Verify initiation of slow dump. Reset PLC Axial Column Force limit to 16,000 lbf.
6. Reset the MPS. Set PLC Radial Column Force limit to 0.1 lbf. Verify initiation of slow dump. Reset PLC Axial Column Force limit to 7,500 lbf.

FAST DAQ KEEP ALIVE – Slow Dump

7. Reset the MPS. Disconnect Ethernet cable from PXi. Verify initiation of slow dump. Reconnect PXi Ethernet cable.

FAST DAQ TURN-TO-TURN SHORT – Slow Dump

8. Reset the MPS. Fake a turn-to-turn short from the PXi. Verify initiation of slow dump.

AC POWER LOSS – Slow Dump

9. Reset the MPS. Using web controls for UPS, open the contact for relay 1 (indicating a loss of electrical power). Verify initiation of slow dump. Close the contact for relay 1.
10. Verify flagged Jumper has been removed and hard wire interlock restored

Qualifying the Magnet at 140 A

1. Voltage tap circuits, quench protection circuits, pick-up coils, PXi system archiving system shall be operational. Sequence of Events Monitor (SOE) may be operational
2. Verify the jumper on the MPS Control Board is in the right-most or inductive position.
3. Set two Current Limits (1) Newport Controller, (2) PLC Software limit to 145 A. Set the (CEBAF) Power supply Limit to 150 A (higher because of low resolution of read-out)
4. Zero-Out Strain gauge readings
5. Turn on the PXi System, initiating a recording session named by the date and time.
6. Zero the PXi system.
7. Turn on the MPS and reset at a requested current of zero. Using the soft ramp.
8. Ramp to 30 A using the soft start ramp.
9. This ramp validates the ability of the hard wire and PLC QD to operate under the soft ramp conditions.
10. Verify that the PXi inductive voltages recorded match the inductances anticipated.
11. If the ramp causes QD trips, or voltages are not as anticipated, debug the systems until success.
12. Ramp to 140 A using the soft ramp.
13. If the ramp causes QD trips, debug the system until success.
14. Observe the following for odd behavior:
    a. Hard wire Quench Detector error signal,
    b. PLC Quench detector signal noise behavior,
    c. Support column strain gauge readings,
    d. VCL voltage and temperature readings,
    e. Voltage tap readings during ramp and at flat top,
    f. Monitor LHe level and valve position history looking for increased usage,
    g. If necessary, follow-up with de-bugging and additional ramps.
15. The final ramp shall remain at current for 20 minutes.
16. Ramp down to zero current using the soft ramp.
17. Observe the following for odd behavior:
    a. Hard wire Quench Detector error signal,
    b. PLC Quench detector signal noise behavior,
    c. Support column strain gauge readings,
    d. VCL voltage and temperature readings,
    e. Voltage tap readings during ramp and at flat top,

f. Monitor LHe level and valve position history looking for increased usage,
g. If necessary, follow-up with de-bugging and additional ramps.

18. Turn off the MPS.
19. Stop the PXi archive and reduce the archive rate of the PLC data.

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Voltage Tap Pair	Tap Coil	Positive Terminal TS-IDB310-1	Negative Terminal TS-IDB310-1	Tap Coil Positive Threshold (mV)	Tap Coil Negative Threshold (mV)	Coil Channel 1 Positive Threshold (mV)	Coil Channel 1 Negative Threshold (mV)	Coil Channel 2 Positive Threshold (mV)	Coil Channel 2 Negative Threshold (mV)	Coil Channel 3 Positive Threshold (mV)	Coil Channel 3 Negative Threshold (mV)	Signature	Date
VTT3	Pos. Lead	2	4										
VTT4	2A	4	5										
VTT5	2B	5	6										
VTT6	2C	6	7										
VTT7	2D	7r	9r										
VTT8	1AB	8	11r										
VTT9	1C	11	12										
VTT10	1D	12	13										
VTT11	1E	13	14										
VTT12	1FG	14	17										
VTT13	3A	16	18										
VTT14	3BC	18	19										
VTT15	3D1	19	20										
VTT16	3D2	20	23										
VTT17	4AB	22r	24r										
VTT18	4C	24	25										
VTT19	4D	25	27										
VTT20	Lead	26	27r										
VTT21	Neg. Lead	27r	28										