12GeV Trigger meeting notes:

22 April 2011: C. Cuevas, N. Nganga, B. Moffit, S. Kaneta, J. Gu, A. Somov, J. Wilson, E. Jastrzembski

15 April 2011: C. Cuevas, B. Raydo, N. Nganga,. B. Moffitt, S. Kaneta, J. Gu; A. Somov, J. Wilson

1 April 2011: C. Cuevas, B. Raydo, N. Nganga,. E. Jastrzembski, B. Moffit, H. Dong,S. Kaneta, J. Gu; A. Somov, J. Wilson

25 March 2011: C. Cuevas, B. Raydo, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu; A. Somov, J. Wilson

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0. Trigger/Clock/Sync – TI/TD

22 April 2011

--> Two crates are configured in the EEL109 lab and William and Bryan have completed the procedure to remove the fiber optic cable delay (skew) between the crates. The two trigger signals were captured on the O'scope and at some point soon, it would be a good idea to go through the zero delay adjustment procedure again, so that others can become familiar with the setup.

-->See SD section for additional discussion, and also notes in the 'customer' section for the status of the FADC250-V2 units that will be installed into these two EEL109 crates.

15 April 2011

→The 2nd VXS crate will be installed next week (Monday) and the 2nd TI, CPU and SD can be installed and configured. We will use the 50m fiber through the patch panels and prepare for the initial FADC250 unit. This will be a perfect opportunity to execute the setup procedure for removing the 'skew' from the different TI fiber lengths.

→No change to the initial single crate setup, and configuring (adding) another ROC should not take too long.

1 April 2011

A TID and SD have been installed the EEL109 VXS DAq crate. A 150m fiber has been connected from TI-port 5 to TI-port 1 through the patch panel and fiber patch cords. The number of tests that can be performed with these two boards is not too large, and a payload test board can be used to monitor clocks and other signals that are driven by the SD board. The status of the firmware for the TI and SD is complete for now, and Bryan can continue testing the library functions for each of these boards.

25March2011

TID is ready to be installed in EEL109 test rack. William has updated the TI-D manual and has included detailed explanation of the fiber skew offset and compensation 'procedure' to maintain zero skew between each front end crate. The skew can be controlled to 4ns.

Latest manual has been updated and posted. Pre-production parts will need to be ordered, and also order for front panels can be released.

2. *SUB-SYSTEM PROCESSOR (SSP)*

22 April 2011

No report from Ben, but it was suggested that a sub-group should meet and discuss the initial implementation plan for using the SSP with the two CTP that will ultimately be used to generate the readout trigger signal to the TI (TS) module. The implementation will have limited programmability and will effectively combine the trigger information from the two CTP. There

will be significant firmware work to implement this by the time we have two crates of FADC250, so now is the time to discuss the details.

15 April 2011
→Ben will complete a register map for the SSP that is specific to this two crate test. Bryan will have to build a driver for the SSP, and clearly it will not be the final revision. The SSP will be used to collect the summing information from the two crates and provide the final trigger signal to the TI that is running in TS mode.
→Ben and Hai have not finalized the transmission scheme for the CTP to SSP link, and next week will hopefully be a good opportunity to review this topic and begin the firmware effort.
→Ben will order a few MTP fiber optic jumpers and we should include fiber links from the CTPs to the SSP.

1 April 2011
Ben reported that he is at the stage of reviewing the details of the transmission protocol/scheme for the link between the CTP and the SSP. 4 bonded Aurora lanes @2.5Gp/s was the method used in 2009, and this will have to be reviewed. Hai will be ready to work with Ben on the CTP->SSP link firmware after work for the FADC250 is running flawlessly.

25 March 2011
No report

3. CUSTOMERS

22 April 2011
-->Bryan has at least one of the FADC250-V2 boards with the latest 'Hall D' firmware revision and Ed has provided an update to the register map document so the iterations to the CODA software libraries can be completed.
-->During the week of 25-April, at least one FADC250-V2 module should be running in the EEL109 two crate test station, and hopefully we can proceed with the second unit as soon as the Detector Group returns the module.

15 April 2011
→Even though Ed and Hai were not present, they demonstrated on Thursday, a fully functional FADC250-V2 running with the latest firmware and with a CTP. Only one channel was used to create a 'sum' and the rate of the trigger was over 1 KHz. The plan is to move this board to the EEL109 lab and begin checkout with the other boards. Ed will update the register map document and Bryan can begin the modifications to the driver.
→Once the 2nd crate is configured we will need the FADC250-V2 that was loaned to the Detector group.

1 April 2011 (Not an April Fools)
Ed reports that the FADC250 board has been tested and that the data format and other firmware features are working. Hopefully we can use at least one of the version 2 boards for initial testing with the SD, TI and CTP in the EEL109 DAq crate. The FADC250-V2 that was loaned to the Radiation Detector and Imaging group should be returned and loaded with the latest firmware so that we can begin populating the 2nd DAq crate.

25 March 2011
Breakthrough on testing and troubleshooting located the firmware issues. Further testing continues. Boards ordered, assembly needs signature from HallB. Secondary order is progressing, need to check parts kit.

4 "B" Switch - Signal Distribution Module (SD)

22 April 2011

-->Nick presented a few oscilloscope photos that showed the clock signals in relation to one another from both crates. There was a good discussion on why the second scope trace exhibited a somewhat significant jitter with relation to the first. Nick also showed a long term, (>8hr) photo from the O'scope that had acquired signals in infinite persistence mode. The two signals did not appear to have any significant variation which shows that the clock signals are definitely phased locked and show no clock cycle drift.

-->Nick mentioned that the SD parts kit is close to final and that the front panels were ready for machining. The files for manufacturing the final pre-production boards are virtually complete and pending final review and performance results from the two crate test.

15 April 2011

The 2nd SD will be needed for when we install the second crate. We do not have a spare SD so any changes to firmware that may be required will have to be kept at a minimum. Nick reports that the front panels for six more boards have been ordered, and that Mark will finalize the parts kit to build six more SD as soon as all testing is complete, and ECOs are verified.

1 April 2011

For the time without a FADC250-V2 board, we can use the payload test board to send a trigger signal to the SD and pass this signal to the TI. Nick has been busy with final firmware changes and has also started to implement the ECOs for the final board design. The components for six SD boards have been received and assembly of the parts kit has started. Soon after the two crate DAq testing, we can send the order for a six board assemblies. The front panel drawings should be checked and ordered now.

25 March 2011

It all works! BUSY discussion and details of other functions need to be coded.
Token
Busy
I^2C working
PLL working
SD-TI "link"
Trigger Hit Pattern block
Counters (Scaling various signals)

5. System Diagrams & Test Stand Activities

22 April 2011

-->No significant update on the draft fiber specification for the trigger signal distribution for the halls. The specification will need to be completed before the end of May to establish a pre-procurement plan for fiber purchase/assembly/installation and testing.

15 April 2011

→The trigger system fiber optic specification will be created and sent for comments soon. It is not clear when these fiber trunk cables and patch panels will be installed in the hall. Finishing the specification and installation requirement document makes sense to complete now, and at least when the procurement begins, the items will only need to be ordered. Fortunately, there are several commercial sources for the fiber and patch panel equipment.

1-April 2011
Start a pre procurement plan for Hall D to include fiber trunk installation and testing. Patch cables and patch panels will be ordered separately.

25 March 2011
Re-work the price estimate for only installation and cost of the 144 fiber trunk lines.

18 March 2011
The initial price quote received for the MTP trunk Fiber and supporting peripheral hardware is surprisingly high. The company included assembly, installation and testing of the MTP trunk fiber cabling for the Hall D example. The company assumed that the trunk cables would be all the same length, but in fact the trunk cables for the Hall will be much shorter, so the cost would also be reduced significantly. On further review, the jacket of the trunk and patch cables can be rated lower than plenum or riser, and this specification will reduce the overall cost further. All said, another price estimate will be generated.

5. Two Crate DAq test configuration

22 April 2011
-->Ed and Hai have completed the final firmware revisions for the initial FADC250-V2 boards and at least one unit should be installed in the EEL109 lab for an initial test with the TI and SD module. Continued progress, and it will not be long before we have two full front end crates!
-->The main goals of the two crate test are extracted from past meetings as follows:
The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:

- **-Verify clock distribution through TID->SD and measure jitter to front end boards**
- **-Verify trigger rate and readout rate for a variety of occupancy levels.**
- **-Verity token passing scheme**
- **-Verify CTP operation with sixteen FADC250 @2.5Gbps per lane**
- **-Test playback mode feature on two crates and verify operation with SSP.**
- **-Measure and record overall trigger latency. (Could include SSP)**
- **-Verify full 2eSST readout from all payload modules**
- **-Verify TI-D features and use one TI-D in TS 'mode'**
- **-Synchronization testing. Quantify number of out of sync events, clock counters etc.**
- **-I am sure there are more milestone tests, but we can iterate the list.**

15 April 2011
→See 1st section, but the good news is that the FADC250-V2 is ready to be installed in the 1st VXS crate. Achieved the new deadline, and we will configure a 20 slot VXS crate that has an ELMA backplane for now. There will be a slight delay for the delivery of sixteen more VXS crates, but we can use the ELMA crate to continue progress with the testing.

1 April 2011
TI-D, SD, Linux ROC, are **installed in the EEL109 lab!!** 150m fiber with patch panels installed also. We will need a FADC250-V2 as soon as possible**!** At least one FADC250-V2 will be ready by 15-April!

The clock phase alignment procedure has been completed by William, and the adjustment for clock phase alignment between front end crates is one 4ns clock cycle.

25 March 2011 (This is in red because we missed the goal!)

Major components for the two crate DAq test are installed in EEL-109. Still need another VXS crate, and the boards will have to have the latest firmware revisions loaded and ready.

*We plan to have at least one crate running with the CPU, TI-D, SD and CTP **by next meeting**. If we can get one of the FADC250-V2 boards, that would be a bonus*.

18 March 2011

Major components for the two crate DAq test are installed in EEL-109. Still need another VXS crate, and the boards will have to have the latest firmware revisions loaded and ready.

We plan to have at least one crate running with the CPU, TI-D, SD and CTP by next meeting. If we can get one of the FADC250-V2 boards, that would be a bonus.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)

So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

   The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

   Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

6. Crate Trigger Processor (CTP)

22 April 2011

-->As stated in a previous section, the plan is to use the latest CTP in the two crate test and verify full functionality with two lanes at 2.5Gb/s from each payload slot. We *should* use the CTP that have the Virtex V FX70T FPGA and increase the serial lane transmission to 5Gb/s AFTER the initial testing is complete.

-->Details of the CTP to SSP data transfer technique will have to be settled sooner than later, so plan on meeting a few times for informal discussions on the best way to implement these techniques in firmware/software.

15 April 2011

→No report but Hai will meet with Ben to arrange a method to transfer the summing information to the SSP. I believe all four CTP are working, but it is not clear which units have the latest firmware. It would be best to use the CTP that have the 'FX70T components, but this is not absolutely required. Will check with Hai next week for the latest status.

1 April 2011

→CTP 1 and 2 will be used *initially* in the two crate test. These units use LX110T and will have the transceiver selection *hardcoded* in the FPGA for a single FADC250.

→For the **final** two crate configuration with 16 payloads we will use CTP 3 & 4 that are assembled with the FX70T part. We will need to have the CTP firmware developed so that each of the Gigabit transceivers can be disabled or enabled. If there are counters (scalers) that need to be added, these must be defined now.

→The ECO list for the CTP design is well known, and will need time to implement on the schematics and PCB. These changes include adding front panel I/O and other small circuit corrections. These ECO are in the plan and create a good deal of work to complete before the end of fy11.

25 March 2011

Let's talk with Hai to verify the next step. The latest CTP have V5FX70 parts and the full firmware needs to be loaded into the latest CTP. There are a few functions that need to be added so that the CTP 'lanes' can be enabled/disabled for the full crate test.

What other essential counter functions will be required?

7. GTP and Global Crate Developments

22 April 2011

-->Scott continues with the final stages of routing the external DDR memory and is quickly learning how to use the Cadence routing tools. The GTP is at the stage of final routing and verification of the fabrication files will soon be needed.

-->The final Bill of Materials is also a work in progress and only a small fraction of the components have been purchased and delivered. The longer lead items and expensive items have been received. Very soon, we should consider starting the parts "kit" for the initial prototype build.

-->Time to revisit the schedule and update any changes that will be needed for firmware development and simulation. There will be a significant development period to implement the Ethernet interface and other required features.

15 April 2011

→Scott reports that the routing stage is nearly complete and once the external DDR memory chips and configuration devices are routed, he will verify the BOM and initiate an order for parts.

→Firmware development will begin soon and will be a significant effort considering the board functions and specifications. Considerations for hardware (full functional) test methods will also require development time.

1 April 2011

Scott presented the latest update on the board layout and the routing for the transceiver lanes look very impressive and on one layer and manage sixteen SSP with 2 full duplex lanes! The board routing paths for the memories, and Ethernet interface is a work in progress. The Specctra router routines will need to be developed but the progress is very promising. Ethernet firmware and Nios embedded code will begin when board sent for assembly. Initial code framework has been developed.

25 March 2011

GTP 3D video of an Altium layout

ACTION ITEMS: **Next meeting → Friday 29 April 2011 10AM in F226**