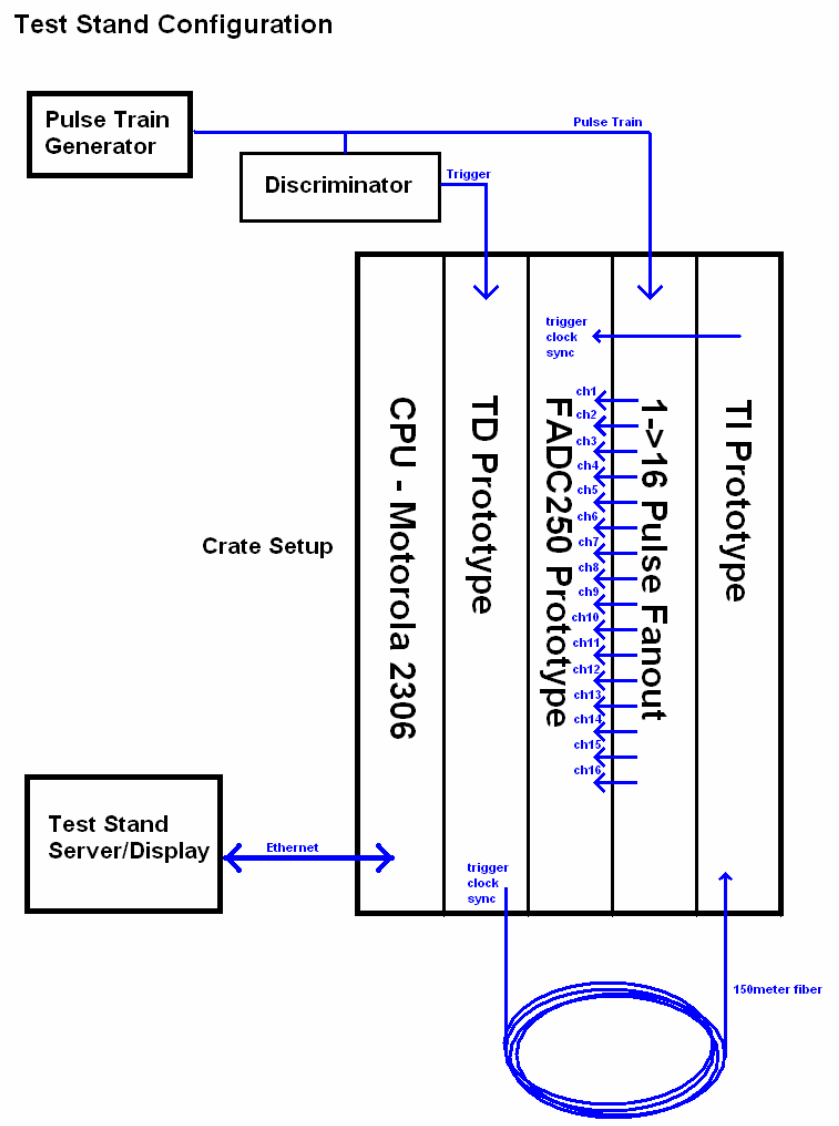
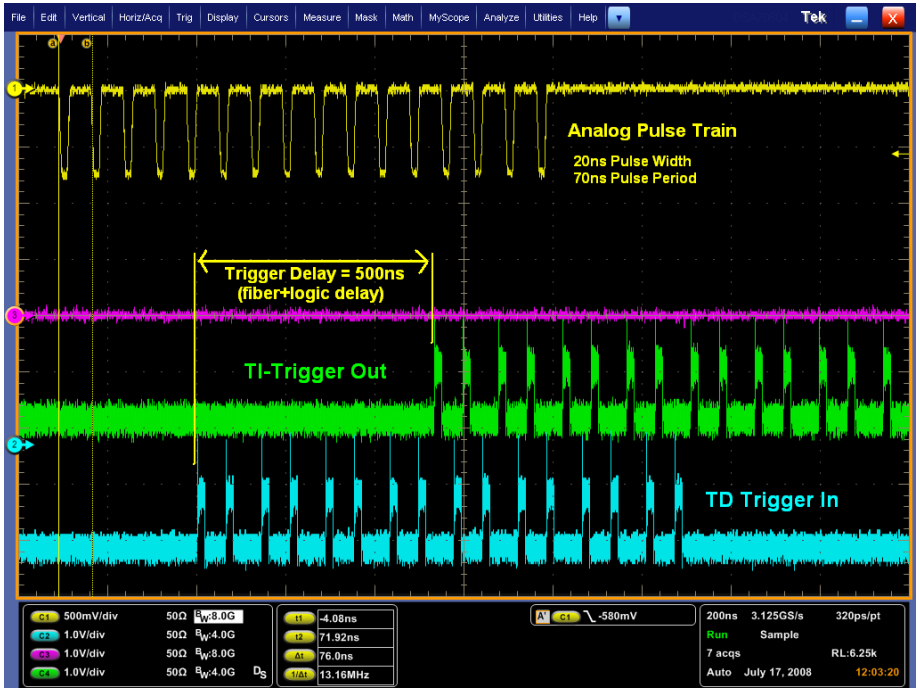
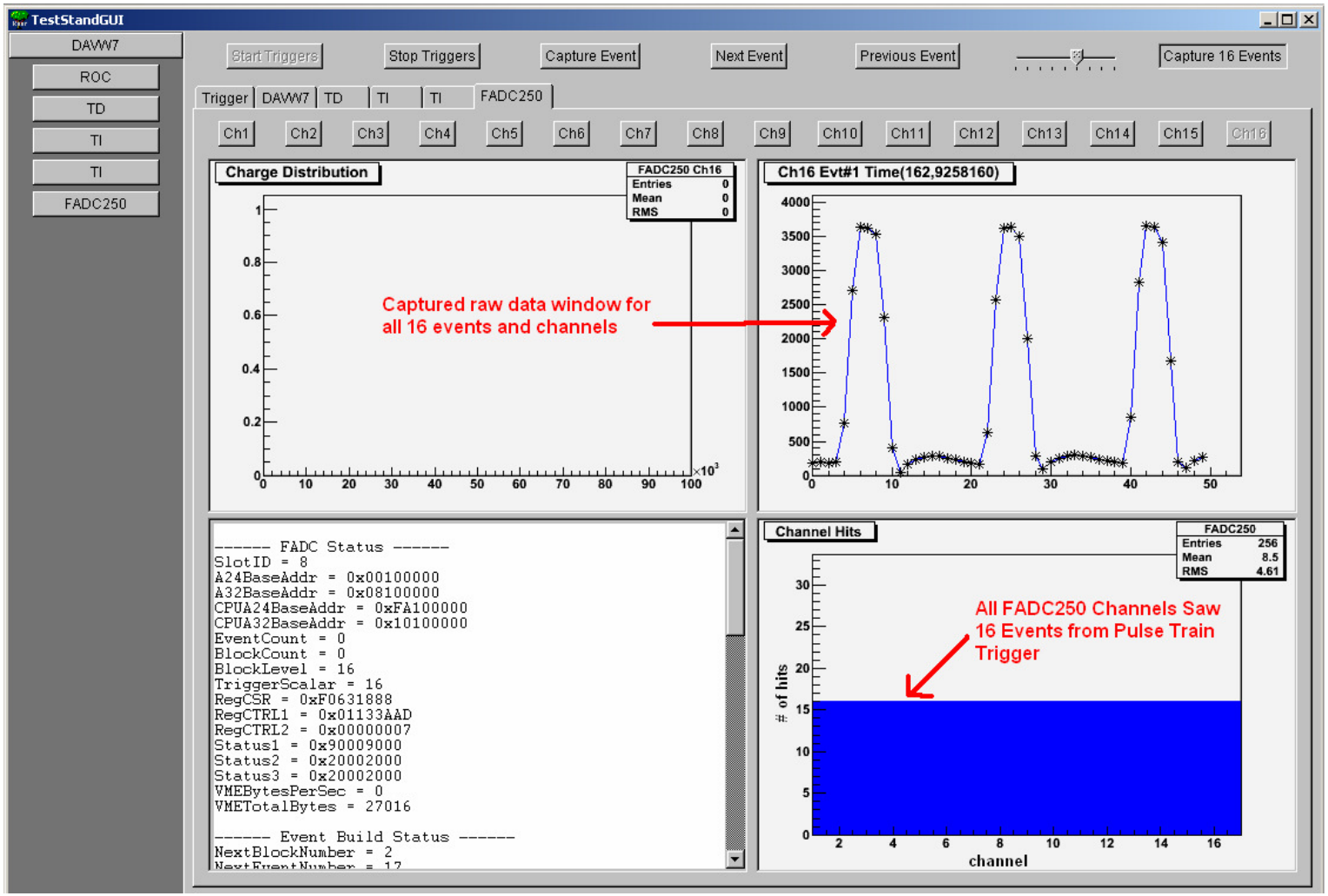
Test Stand Status – Initial Testing



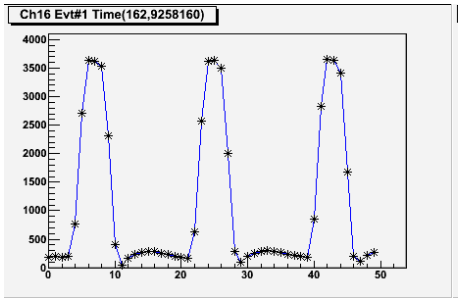
- Used TD, TI Fiber Based Clock & Trig Distribution
- Pulse Train Length of 16, 70ns spaced triggers
- Fed into all 16 FADC250 Channels



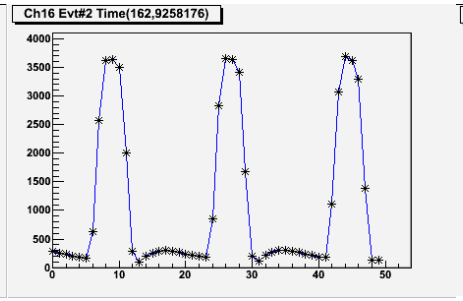
Test Stand GUI FADC250 Tab Display – Pulse Train Event Capture



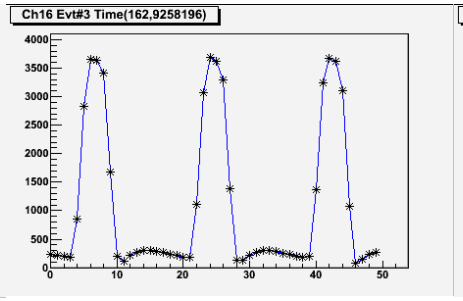
t=0ns, pulses 1,2,3



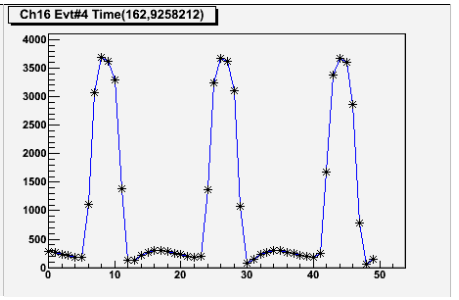
Δ t=64ns, pulses 2,3,4



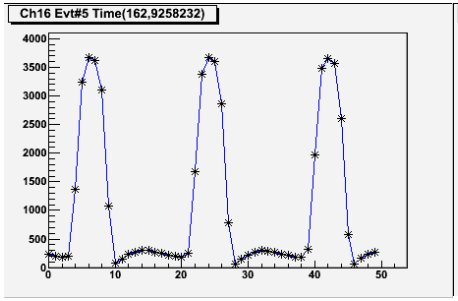
Δ t=80ns, pulses 3,4,5



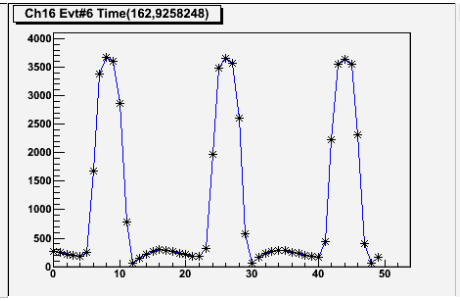
Δ t=64ns, pulses 4,5,6



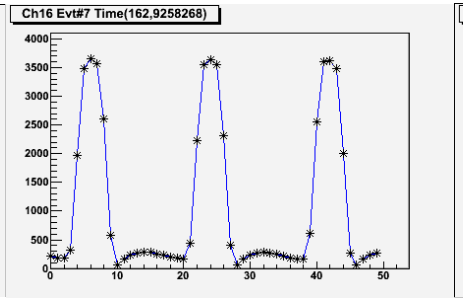
t=80ns, pulses 5,6,7



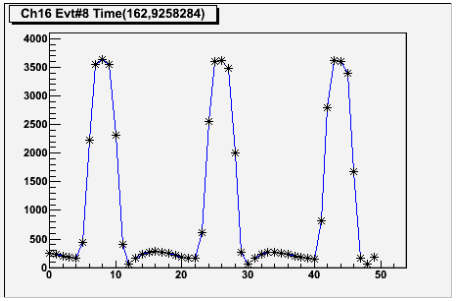
Δ t=64ns, pulses 6,7,8



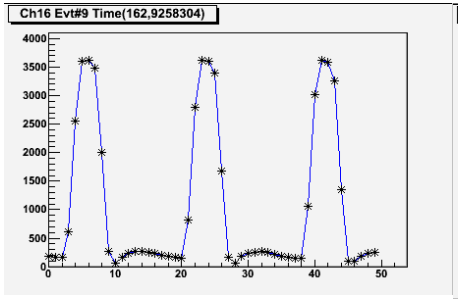
Δ t=80ns, pulses 7,8,9



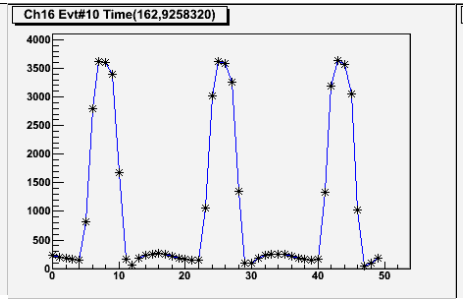
Δ t=64ns, pulses 8,9,10



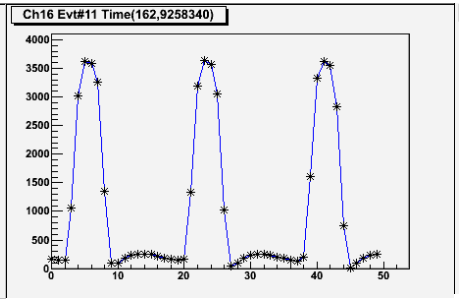
t=80ns, pulses 9,10,11



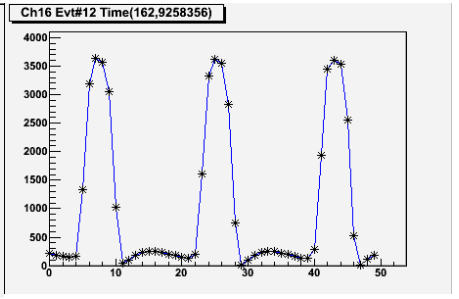
Δ t=64ns, pulses 10,11,12



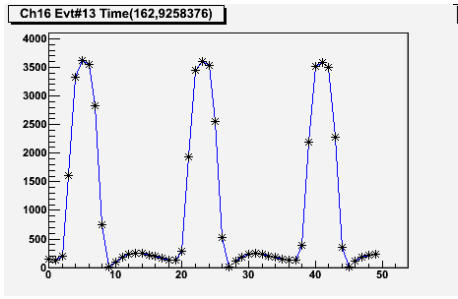
Δ t=80ns, pulses 11,12,13



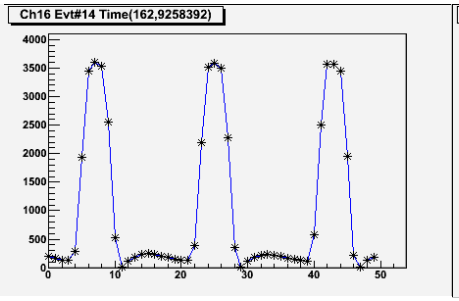
Δ t=64ns, pulses 12,13,14



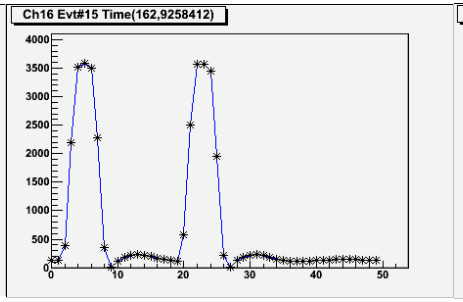
t=80ns, pulses 13,14,15



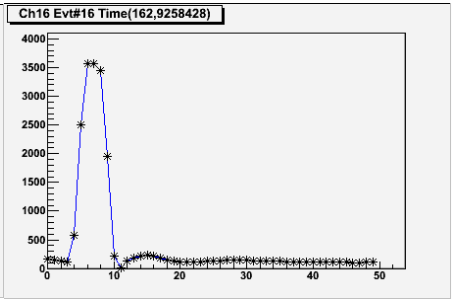
Δ t=64ns, pulses 14,15,16



Δ t=80ns, pulses 15,16

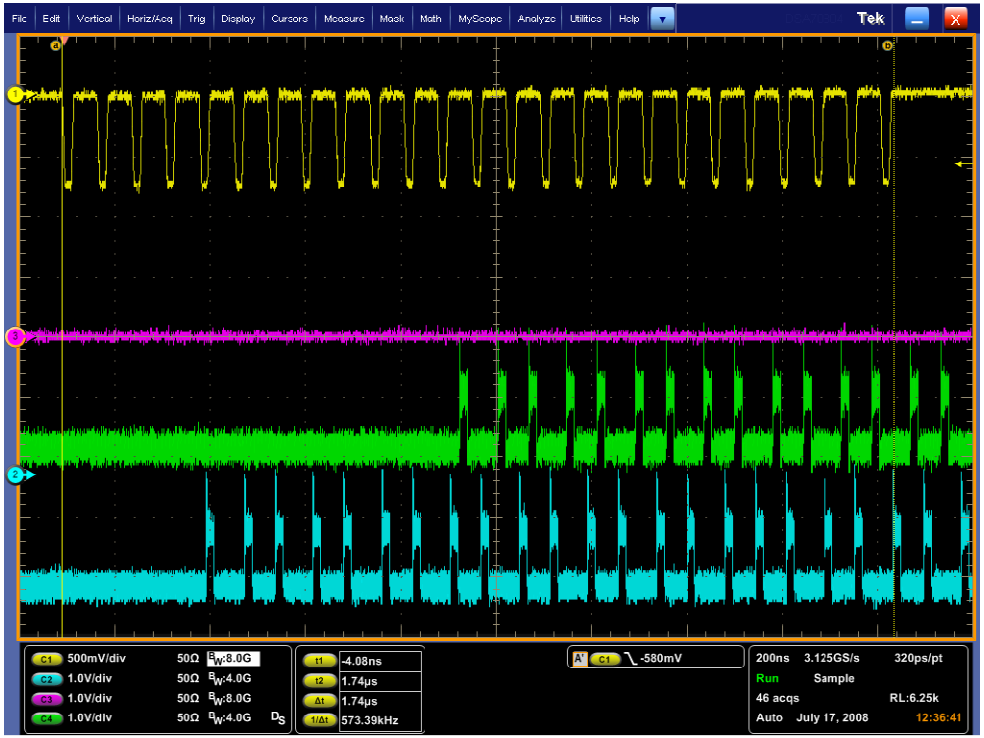


Δ t=64ns, pulse 16



Test Stand Status Summary/To-do

14MHz Pulse Train of Length 25:



- **FADC250 captures this type of pulse train having up to 25 sequential pulses 70ns apart – after this point a bug causes FADC250 to fail - ultimately a BUSY flag will halt the Trigger Supervisor from distributing anymore triggers to prevent overburdening the FADC250.**
- **This test indicates that the FADC250 pulse processing will easily be able to handle a 200kHz trigger rate.**
- **Large signal jitter (seen as 16ns in previous capture) is introduced from trigger distribution. The Trigger Supervisor will remove this by storing to the event stream the precise 250MHz clock cycle a trigger happens.**