12GeV Trigger meeting notes:

16 April 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, A. Somov, J. Wilson

2 April 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, E. Jastrzembski, J. Wilson

19 March 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, E. Jastrzembski, J. Wilson, A. Somov

11 March 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, E. Jastrzembski, J. Wilson

4 March 2010: C. Cuevas, H. Dong, J. Gu, B. Raydo, E. Jastrzembski, A. Somov, J. Wilson

Updated prototype board status table:--21 April 2010

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** **SN001 ----------** **SN002 ----------** **SN003 ----------** **SN004 ----------** **SN005 ----------** **SN006 ----------** **SN007 ----------** **SN008 ----------**	 **Daq Lab F110** **Daq LabF110** **Daq Lab F110** **EEL – 126** **EEL109** **F-Wing Lab** **Hall A** **EEL – 126**	 **Test Board** **OK Hall A Student** **Moller Spare** **FDC test setup** **Needs repair** **F117 (A. Somov)** **Moller setup** **FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded** **Sent to IU for FCAL testing** **12Oct2009** **'64x crate and LinuX Cpu sent 24Jan10**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Modules used for system testing**
5	**VME -- FP-SD** **F**ront **P**anel **– S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete** **Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250!!**
1	**Crate Trigger Processor**	**EEL 109**	**Successful testing with multiple FADC250 and in SSP mode!!**
2	**Signal Distribution**	**EEL109**	**Testing complete**

0. Trigger/Clock/Sync – TI/TD

16 April 2010

William is at the stage of final checking for the layout of the new TI-TD module. The schematics should also be closely checked, and William has created a detailed Bill Of Materials. The initial manufacturing and assembly of the board will be funded from the DAQ group and the FPGAs required for the initial boards have already been purchased from PELEC funds.

William and Ben compared the jitter between two Avago fiber transceivers and the results were virtually identical. The 2.7Gbps part will be used for the TD-TI links and the higher speed transceiver will be used for the CTP-SSP links.

Fiber transceivers for full testing of the TI-TD will need to be ordered, and we will order at least 6 of the higher speed transceivers for the SSP testing.

William has made progress on two other designs in parallel with the high priority TI-TD project. The fanout module for the CAEN V1290 TDC has been defined and is progressing, plus the mezzanine card adapter for the TI-TD is also in progress.

19March 2010

William has provided updates to the schedule for three board projects. The TI/TD module design is progressing nicely and schematics are ready for a check.

The 2.7Gbps transceivers were received and were tested in the lab by Ben and William. Results were not remarkable compared to the 3.125Gbps transceivers, but a few plots of the results would be useful. These components would save some costs for the TI-TD fiber links.

As soon as a BOM is created for the prototype TI/TD, any long lead items should be ordered.

4 March 2010

The TI/TD and two other board designs for the distribution of global trigger signals are on schedule and William has updated his schedule progress.

The 2.7Gbps transceivers were delivered and should be tested soon to see if the intrinsic jitter performance of the clock distribution is significantly different than the 3.125Gbps components.

The cost savings to use these transceivers was shown at the last meeting; however, we should plan to use the higher speed grade parts for the CTP to SSP link because these links can be driven to their full bandwidth by the FPGA on the CTP. The quantity needed for the TI-TD links may be able to use the 2.7Gbps part, but the intrinsic jitter spec is the main concern, and needs to be tested thoroughly.

1. FIRMWARE TESTING

16 April 2010

→A few iterations to the Playback mode have been completed, and Dave Abbott has started to add the new "Playback" mode to his existing FADC250 library. These functions will be eventually used for system commissioning and test. This "Playback" feature will be very useful to test and troubleshoot the entire trigger system. It might be a good time to draft a full description of this "Playback" mode including an implementation plan.

→PREx is off to a successful start and the Moller firmware has been in use for some time now. It would be interesting to see the results from the experiment data.

→Firmware design and testing is close to completion for Ed's full conversion of the AHDL to VHDL for use on the latest revision of the FADC250 and this firmware can be used for future VME module designs.

19 March 2010

→Hai has completed the "Playback" mode for the FADC250 that will create a waveform in local memory and continuously run these waveforms from the front end FPGA so that the triggering functions upstream can be tested deterministically. The firmware can be tested as soon as reasonable and will be loaded onto the board that Alex is using. The firmware documentation has been updated to include the playback mode.

→Ed reports that the VHDL firmware is complete and will need to be tested on a module for full verification. Ed reports that there is some discussion of adding a big endian-little endian control to the readout word so that the new Intel based CPU does not have to swap the bytes. This issue was raised by Gerard and will be implemented on the FADC125.

4 March 2010

Ed reports that the converted AHDL firmware is virtually complete and is in the final stages of testing. As mentioned at previous meetings, the new firmware can be loaded and tested on different boards to measure performance.

No new updates to the FADC250 code lately, and the PREX folks will be running soon and experiment data will be collected from the flash board in Hall A. The Moller firmware was completed many months ago.

2. ***SUB-SYSTEM PROCESSOR (SSP)***

16 April 2010

→The SSP is at the stage of checking manufacturing files and final review of all schematic and design rule checking. Considering the complexity of this board and the number of layers, it is prudent to verify and check the design before ordering the initial board. No significant issues to report here regarding the Altium –to- Cadence Specctra routing, and Ben has provided a significant amount of work to keep this project on schedule.
→All components for the initial SSP have been ordered. We will order the fiber transceivers soon.

19 March 2010

Ben is preparing to route the SSP with the Specctra router and will configure a quad core machine in the lab for this purpose. The new computer center rules for putting machines to sleep can be bypassed, and if a machine is busy, then the computer center sleep routine will wait until the machine has completed a routing job.

The BOM should be available and long lead items identified!! Consolidate where appropriate and prepare an order before the end of the March!!! Chris will locate appropriate cost accounts for these prototype quantity purchases.

4 March 2010

Ben updated the latest status with the SSP design, and the global trigger crate pair mapping was updated to reflect the latest SSP design. There will be a significant level of work required for the board routing process and hopefully we do not run into any contentions for the Specctra router key.

Parts is parts, and I will say it again that I think the long lead items need to be ordered by the end of March! Even though it is not a large order, I think consolidating the order for long lead parts for the FADC250, SSP, and TI/TD makes sense. These parts will be funded by 12GeV.

3. CUSTOMERS

16 April 2010

→PREx in Hall A is running!
→IU FCAL group is finished with the 12 bit FADC250. Not sure if they will send that unit back to Jlab soon, but the last email I read indicated that they had collected plenty of data with the new timing algorithm and have produced a paper with the results.
→One FADC250 has been reserved for the JLAB Injector group for their upcoming Compton and Mott applications. They will need a test crate and supporting peripheral level translator for the trigger input, and the hardware has not yet been transferred to them. Contact: Joe Grames
→Table 1 has been updated and the 9 prototype FADC250 units have been stable and in use for close to a year without significant problems.

19 March 2010

→Sasha will implement and test the new “Playback Mode” with the FADC250 in the F117 lab. This will be an opportunity to verify the triggering functions of a module and also lead the way for system level commissioning of each crate and associated global trigger modules.
→No recent news from the PREx folks in Hall A and this week they will receive beam and proceed with the commissioning phase of the experiment. It will be interesting to see their results.
→The 12bit FADC250 that is in IU with the FCAL folks may be able to be used by the TOF folks in Florida. The decision to send a flash board to Florida has not been made yet, but I anticipate that they will need a module after they record measurements of their phototubes and scintillation counters.

4 March 2010

→Sasha described his recent success and setup with the FADC250 board he has configured in F117. The plan is keep this board for continued testing and development of the front end "data playback" mode that will be used to commission the trigger system. Hai has started a specification document that describes the 'data playback' mode that includes an implementation plan.

→No news from the IU FCAL group regarding the latest measurements using the 12bit board.

→Request from the Florida State TOF group was answered, but it is not clear what they will need for their test setup. It is clear that they will need a VXS backplane, but the overall goals of what their priority measurements need to be has not been described.

4 "B" Switch - Signal Distribution Module (SD)

16 April 2010

→**Welcome to Nicholas Nganga!** Nick has started work and will be assigned to the revision of the SD module. Other projects will be assigned as well, but for now, he will be ramping up his understanding of our trigger system architecture and design specifications for the SD module.

→The final VXS pair mapping has been defined for the front end and global trigger crates. The final mapping definitions have been revised on the FADC250-V2 and of course, the new trigger module designs will use this final pair mapping.

5 February 2010

No new activities planned and modifications to the existing modules will have to take place before testing begins with the latest version of the FADC250 boards and the SSP.

8 January 2010

The SD module will need to be revised to reflect the changes to the signal pair mapping for the front end crates. We have two modules in the lab and I believe we can modify these units to work for testing the SSP prototype and revision 1 of the FADC250 that will be ready before the end of FY10. The SD module revisions are effectively only signal pair changes and there are a few other circuit changes that will also need to be included for the final production lot.

5. System Diagrams & Test Stand Activities

16 April 2010

The time has arrived to discuss the testing activities for the SSP, TI-TD and other system level testing that will be required after these modules have been received from assembly. Many of the test activities will be low level board functionality tests, which will require test crates, and other support hardware.

The activities for developing libraries for CODA will have to be accounted and I believe we should plan for FY11 to implement the next level of 'DAQ System' testing that will be required to test and measure the performance of the readout and trigger hardware in a multi-crate format. We have performed these tests with the ***prototypes*** of the FADC250, CTP, SD and TI and the next level of testing will include more FADC250, SSP and the new TI-TD. I would like to dedicate some time to discuss these activities at the 23-April meeting.

19 March 2010

A brief discussion of the test stand configuration for testing the TI/TD, SSP and version 2 of the FADC250 was started and it makes sense to dedicate a meeting to the activities that will be needed for testing these modules as a system.

4 March 2010

Nothing new to report. Fiber optic layout and details will become a significant project for FY11.

Crate Trigger Processor (CTP)

CTP activities are complete.

6. Projects for FY10

16 April 2010

→No action on the GTP other than an update to the specification and selection of the Xilinx FPGA.

→Details of the testing activities will need to be listed soon, as I suspect there will be a need to order a few essential items to support these new system level tests

→No action on updating the trigger system diagrams for the fiber optic distribution. These drawings must be completed in FY11 and all cable and fiber hardware specified for procurement.

→Full crate test activities need to be detailed

19 March 2010

The projects outlined for FY10 are progressing nicely with the exception of the GTP. The specifications for the GTP have not changed, but a new solution for implementation of the design has been determined. Schematics for the GTP must start soon.

Prototypes of the SSP, and version two of the TI/TD will be completed before the end of this fiscal year and these modules can be tested in concert with the FADC250 version two boards that will be ready also.

4 March 2010

→The GTP update was presented and a single chip solution exists for the GTP prototype. Altium Summer09 has the part in the library so at some point in the very near future a schematic will be conceived. A very big start to this is the fact that the CTP can be copied and many of the same parts re-used. The switch board format is also complete!

→We discussed the use of two GTP for CLAS12 and it is clear that an updated requirement from the CLAS12 folks is in order for the global trigger hardware. GlueX has not requested any new global trigger requirements, so in principle a single GTP should be able to manage the experiment trigger equations. The SD functions for each GTP will remain, and we also discussed that it may be a very good idea to implement at least 4 of the inter-switch pairs for future use.

ACTION ITEMS: **Next meeting → Friday 23 APRIL 2010 at 10:00am in F227**