Implementation of a Level 1 Trigger System using High Speed Serial (VXS) Techniques for the 12GeV high luminosity experimental programs at Thomas Jefferson National Accelerator Facility

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I Introduction

We will demonstrate a hardware and firmware solution for a completely pipelined multi-crate Level 1 trigger system that takes advantage of the elegant high speed VXS serial extensions for VME.

The 12GeV high luminosity experiments planned at Jefferson Lab will rely on multiple VXS Front End Crates for data acquisition and formation of the Level 1 trigger using detector energy summation. L1 trigger rates are expected to be <=200KHz for some experiments.

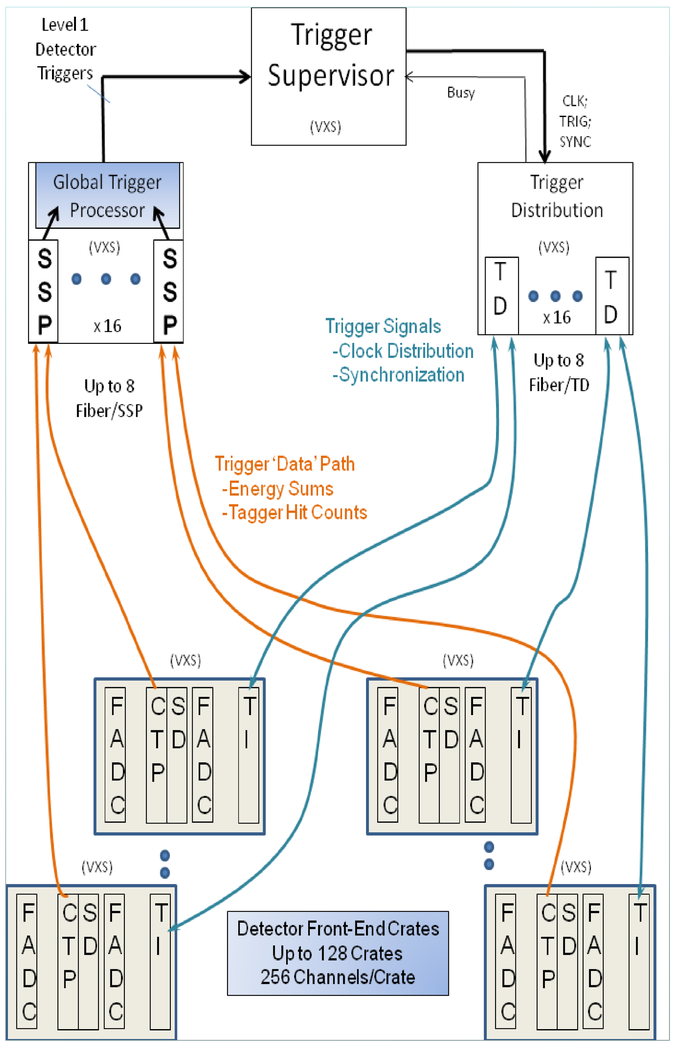
We have designed and constructed several of the essential custom trigger modules and assembled the prototype units in a two crate Level 1 trigger 'test stand'.

II Module Descriptions

- JLAB FADC-250 -- *VITA 41 Payload*
  -16 Channel 10 bit 4ns flash ADCs
  -SUM data transferred using Xilinx Gigabit transceivers. 2 "lanes" @ 2.5Gbps
  -VME SST data transfer mode supported
- **C**rate **T**rigger **P**rocessor (**CTP**)
  -VITA 41 Switch
  -Collects SUM data from up to 16 FADC250 modules within a front end crate
- **T**rigger **I**nterface (**TI**) – *VITA 41 Payload*
  - Receives and manages TRIGGER, SYNC and CLOCK signals from Trigger Supervisor
  -Interface to Crate Cpu **R**ead-**O**ut **C**ontroller
  -Uses Fiber Optic transceiver interface from/to Trigger Supervisor crate
- **S**ignal **D**istribution (**SD**) – *VITA 41 Switch*
  -Receives CLOCK, TRIGGER, and SYNC signals from TI and distributes to FADC250 Payload modules
- **S**ub-**S**ystem **P**rocessor(**SSP**) – *VITA 41 Payload*
  -Receives Trigger SUM data from up to 8 front-end CTP modules via multi-fiber cable

The block diagram below shows a complete Level 1 trigger system planned for the 12GeV experimental programs.

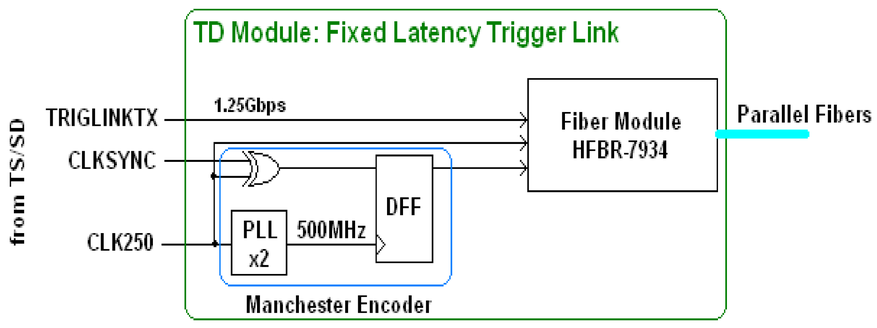
The L1 trigger data path is shown including the Clock, Synchronization and Trigger distribution and trigger supervisor communication link.



III Clock Synchronization, Distribution, and Fixed Trigger Latency

The front-end FADC250 modules demand a low-jitter clock signal and distribution of the 250MHz clock, synchronization signals, and trigger signals. This is accomplished with a Gigabit multi fiber optic driver, careful component selection, and circuit board layout techniques to achieve <3ps jitter.

Front End Crates are located at various distances from the Global Trigger crate, and the time differences are compensated at each crate to achieve a synchronous sampling system and fixed latency trigger time. The Trigger Interface module in each front end crate manage the compensation with the use of a Manchester encoded ClockSync signal.



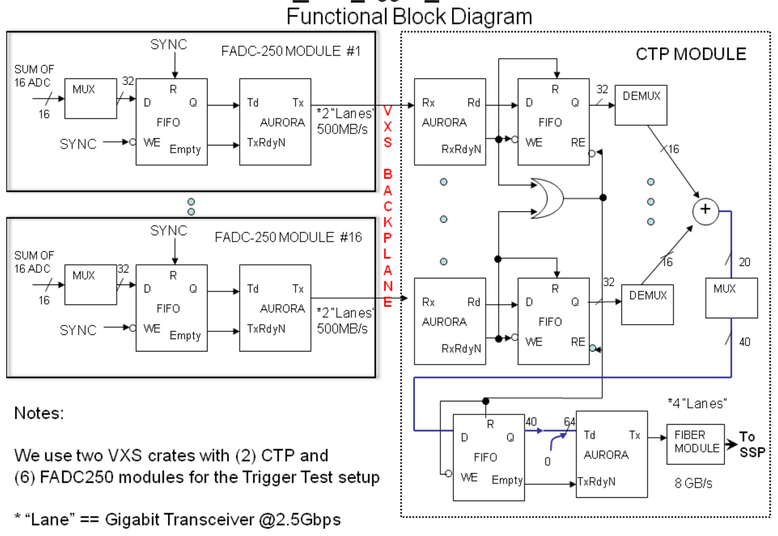
The fiber module is a POP4 compliant 4 channel Rx/Tx fiber module with 4 lanes @ 3.125Gbps per lane using 8b/10b encoding/decoding. This device is compact and can interface directly to Xilinx Virtex V Gigabit Transceivers. We have tested our system with fiber lengths of 50m and 150m to show the performance, and the longest fiber length that will be used in the experimental areas is <150m.

IV Trigger Data Alignment Methods

- **VXS Backplane**

Two lanes @2.5Gbps from each FADC250 *payload* module are transmitted to the **CTP** *switch* slot using Xilinx's Aurora protocol on the VXS backplane. The energy sum transfer rate is 500MB/s from each FADC250 *payload* module to the **C**rate **T**rigger **P**rocessor *switch* module.

Crate **T**rigger **P**rocessor
Functional Block Diagram



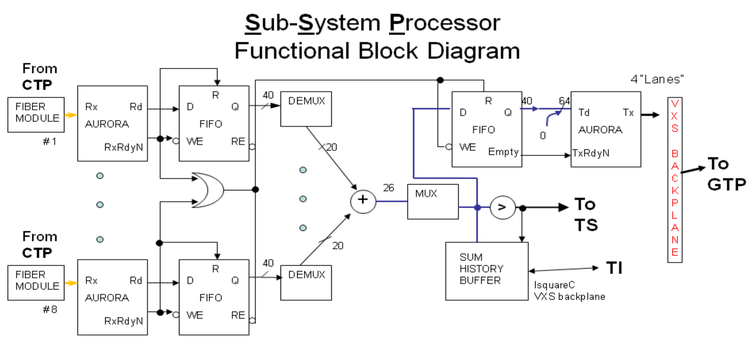
Notes:

We use two VXS crates with (2) CTP and (6) FADC250 modules for the Trigger Test setup

* "Lane" == Gigabit Transceiver @2.5Gbps

- Energy Sum data from each **C**rate **T**rigger **P**rocessor is transferred to the **S**ub**S**ystem **P**rocessor via a multi-fiber optic cable where 4 lanes @2.5Gbps are used for an aggregate transfer rate of 10Gbps. The SSP aligns the data using the method described below:

Sub-**S**ystem **P**rocessor
Functional Block Diagram

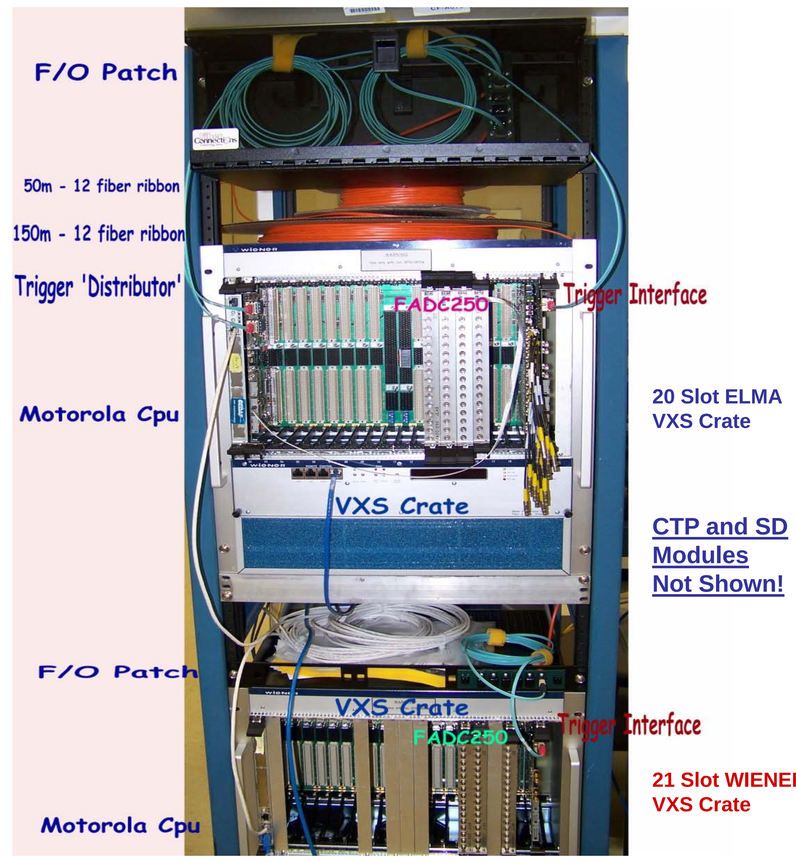


Notes:

We use two VXS crates with (2) CTP.
One **CTP** is operated in **SSP** mode and combines data from one **CTP** via 150m of fiber and the other CTP sums data from two FADC250 in the Trigger Test setup

* "Lane" == Gigabit Transceiver @2.5Gbps

V Two crate L1 Trigger Test Setup

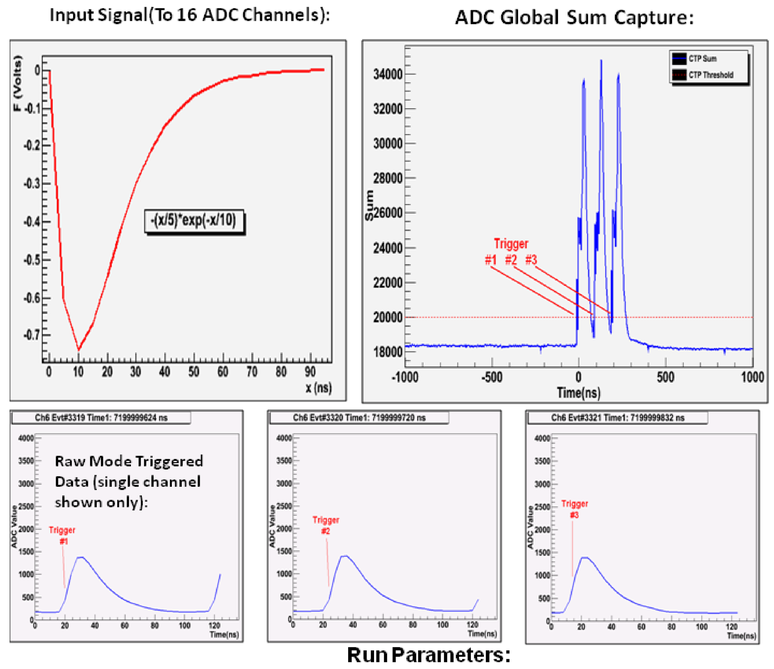


The photo above shows two VXS crates with backplanes from two vendors. We configured 4 FADC250 modules in one crate, and 2 FADC250 modules in the second crate. Both crates use a **T**rigger **I**nterface, **S**ignal **D**istribution, and **C**rate **T**rigger **P**rocessor boards. We use a custom built VME pulse fan-out unit to distribute 16 pulses to the FADC250 modules. These 16 input pulses are summed from each crate, and a trigger signal is created when the total sum crosses a programmed threshold. VME readout is performed using Motorola 6100 controllers in each crate, and we use VME-SST to achieve >110MB/s transfer rates.

VI Results

Our custom designed flash ADC and trigger processing modules function together in a two crate test system that successfully demonstrates high speed digital summing, low jitter precision clock and synchronization plus pipelined data techniques. VME SST has been successfully implemented to read out both 'raw' data mode and pulse charge mode.

Sustained trigger rates of 175KHz at 40MB/s have been achieved, and with minor improvements to the FPGA firmware, we will meet or exceed the 12GeV trigger electronics requirements.



Run Parameters:

Raw Mode: 120kHz trigger rate (140kHz max), 16 hit channels, ~110MB/sec

Charge Mode: 150kHz trigger rate (175kHz max), 16 hit channels, ~40MB/sec

FADC Window Width: 128ns (32 samples)

Input signal: 120-150kHz, burst of 3 pulses separated by 100ns @~40-50kHz

Digitized Sum: 2 crates, 6 FADC, 16 Active Channels

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