12GeV Trigger meeting notes:

13-Jan-2012: C. Cuevas, W. Gu. B. Moffit, N. Nganga, J. Wilson, S. Kaneta, Ed Jastrzembski, A. Somov

9-Dec-2011: C. Cuevas, W. Gu. B. Raydo, B. Moffit, N. Nganga, J. Wilson, S. Kaneta

2-Dec-2011: C. Cuevas, W. Gu. A. Somov, B. Raydo, B. Moffit, N. Nganga

---

0. Trigger/Clock/Sync – TI/TD

13Jan2012

-->TS 1st article board will be assembled and delivered in a few weeks. Acceptance test firmware in development.
-->TI-TD procurement has started and is approved. Accessory orders have been placed, and production quotes have not been received or evaluated yet. Accessory items are front panels, F/O Transceivers, and alignment pins.

Last week a discussion of consolidating the global crate to include SSP, GTP, SD, TD and TS was held and several issues have been identified. I believe there is an issue with the serial transmission of the trig1 and trig 2 signals from the TS to the SD, but other than that, this configuration should work.

9-Dec-2011

-->Specification and BOM in progress for the production order.
TS Trigger holdoff/pulse width settings, etc. How does this need to be specified and handled in the full system. A few timing diagrams may help define this. Minimum trigger pulse separation is 60ns.(FADC250)
→TS 1st article board has been ordered. Two parts: PCB and assembly. Delivery by Feb.

2-Dec-2011

→TS 1st article PR has been submitted and is in process for ordering. This will be a consignment order, because we have the components for a single TS board.
→List results from TI clock meeting held on Wed 30 Nov.,,,,

1. *SUB-SYSTEM PROCESSOR (SSP)*

13Jan2012

SSP "pre-production" could be advanced and initiated by summer if folks have a need for a few boards for evaluation/testing. There are a few groups that would like to use a SSP so maybe this makes sense. Minor circuit ECO will be completed before this pre-production run.

Final production order will be placed in August -2012 and will coincide with installation of crates and other infrastructure that will be needed before pre-commissioning can begin in the halls.

Development activity for the HPS test run in March-2012 will include firmware for the SSP, and a requirements document is in place for the new firmware required for the FADC250. This is a very aggressive schedule for the March run, but a goal has been set.

2. CUSTOMERS

13Jan2012

-->The production order for FADC250 has been awarded and the production orders for the SD and TI-TD boards is in procurement waiting for bids. We have started discussions with the

Accelerator group and MIS to use a common database tool to manage the volume of different DAq boards that will be used in all of the halls. This tool is a work in progress, but will handle all equipment tracking and repair information.

9- Dec-2011
Online database tool at the conceptual stage. We will have a fairly enormous quantity of boards and different boards to track, so a tool will be needed to handle this problem.

18-Nov-2011
→FADC250 boards, SD boards, TI boards and CTP are used by several 'customers".

- Hall B – Inner Calorimeter – Full crate, SD, CTP and TI
- Hall B – Hall D FCAL test – FADC250, SD, TI
- Injector Group: FADC250

→A fairly large batch of VME FADC250 fan-out modules have been ordered and are in the assembly process. Should be able to release a few boards to Alex, and Sergey by 5-Dec.

3. "B" Switch - Signal Distribution Module (SD)

13-JAN 2012
Signature approvals for the production order is 50%.
PRs for accessory items needs to be submitted. Accessory items are front panel, and alignment keys. This PR can use the same account codes and quantity breakdown.
Nick has created a test plan document, and will need to modify and update this test procedure in preparation for the 1st article production test acceptance and production unit testing.

9-Dec-2011
→PR for the SD is in progress.
Specification is complete
BOM complete
Manufacturing files complete
Will need specification signatures and account number approvals before sending to procurement.

2 Dec 2011
No report but the PR will be signed and submitted by the time Nick

18 Nov 2011
→Production order specification and BOM files are a work in progress. Goal is to have a PR created in the system to begin the contract by the time Nick goes on vacation.

4. System Diagrams/Fiber Optics

13JAN2012
Peripheral components can be purchased now for the trigger fiber optic system. For example, the patch panels and patch cords can be purchased. The trunk fiber cable will not be purchased until the cable trays and platforms are in place, so that an accurate length can be given to the selected vendor. Looking at the schedule, these length values for the trunk cables will be ready by summer 2012.

December 2011
No update to draft specification status. Procurement is not critical until first quarter of FY12. System level drawings have been updated for both Hall D and Hall B to reflect the latest requirements for the parallel fiber optics that will be used for the trigger hardware.

5. Two Crate DAq test configuration

13-Jan-2012

-->Chris will draft a "Full DAq Crate Test Procedure" document. The idea is that all boards in a single crate will have passed individual acceptance testing and these boards will need to be operated in concert with CODA and together in a VXS backplane to verify full readout and synchronization testing. This will eliminated full crate troubleshooting in the halls.
-->Random pulse generator testing with playback data needs to be documented.
-->Need to get started with configuration and test goals for the global trigger crate testing. We will have ALL custom trigger boards in either production or 1st article format by March, and can begin testing the SSP, GTP, SD, TD and TS in a full crate. Needless to say, significant CODA driver library development activities will increase.

9-Dec-2011

→Discussion on global trigger hardware testing
BER test? Need to do.
Test in lab using a random pulse generator to start the playback data. Perform the same testing as before and measure trigger rate vs. CPU transfer rate.

2-Dec-2011

→Production testing – Full crate with CODA – Make a goal of Feb-2012 to have a prototype setup of this test station in place.

18 Nov 2011

→Bryan has been testing hardware with the EEL109 crates using the remaining modules that have not been deployed to “Customers”. A new bug has been identified with the TI at high input trigger rates.
→Set up a test for BER would be a very good measurement to record, and this would need at least a few days of dedicated running to establish a realistic test. Need to discuss further.

11 Nov 2011

-->Hai and Bryan have successfully tested a full crate using playback mode. The summing information from each FADC250 payload board has been aligned properly in the CTP to create the crate sum.
→The GOALS of the two crate test station have been successfully achieved and the amount of work is commendable.
→The number of available FADC250 boards is diminishing, but we should set up the two crate EEL109 test station for a long term BER test using as many boards as possible.
→Creating a draft procedure for a full crate test using playback mode and CODA would be brilliant and would allow other personnel to perform full crate acceptance testing. Typical questions, Who, When, What priority?

3 June 2011

→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
See older note dates for the list.

6. Crate Trigger Processor (CTP)

13-Jan-2012
Discussion about how to proceed with the FY12 order of production boards for Hall D. Existing version meets(exceeds?) requirement for energy summing and other parameters. Goal is to order production units by 1-Aug-2012.

Will continue to work with the CLAS12 folks for a written requirement document to justify a new design for the CTP. The new requirements for the CTP may in fact affect the design of the SSP, so this will have to be discussed in detail. Schedule impact will be a significant issue to consider.

9-Dec-2011
→Conversion of CTP-2009 (PCAD) to Altium 2012 will happen today!

2-Dec-2011
→Conversion of the PCAD CTP database to Altium will be complete by 5-Dec-2011. Review required ECO and other circuit additions. Goal to fabricate production boards by Q4-FY12.

7. GTP and Global Crate Developments

13-Jan-2012
-->Scott continues to make progress on the Ethernet development, and will complete testing of the FO transceiver soon. Some work activity will be completed by Scott for the upcoming HPS run and we also discussed activities to verify the limits of the FADC250 to CTP Gigabit serial speed. (Works at 2.5Gb/s but hardware limits need to be tested @5Gb/s). Scott can use a FADC250 and the GTP to document results of the higher speed transfer.
9-Dec-2011
→Ethernet development in progress.

18-Nov-2011
→Need to review the requirements/specification document for the GTP and focus on the primary functions. The Ethernet interface will need to be completely defined soon so that any software development tools/licenses can be accounted and purchased this year.
→Not too early to begin creation of a Global Trigger Test document that will include SSP, TS and SD.
→Trigger equations: What other required features for the GTP are needed?
-Minimum Bias Trigger
-Cosmic Ray Trigger(s)
-Diagnostic Trigger(s)

11 Nov 2011
-->Testing continues: DDR memory, power, and several other hardware functions have been tested.
→Ethernet development has started, but details need to be defined.
→Investigate how to make the GTP appear as a ROC; (Cmsg). Investigate does not mean implement, but Scott needs to know the requirements for the Ethernet interface.
→Physics equation was loaded into the GTP Altera FPGA and Scott presented the latest results for the latency through the part.

- Altera design approach used 46 clock cycles (184ns) to perform the final GTP equation that was initially tested with the Xilinx FPGA.

→Prepare a test plan for the global trigger crate. (SSP, GTP, SD, TI, TS?)

ACTION ITEMS:Next meeting -Friday 20 JAN@ 10AM in F226