
**Nuclear Physics Division**
***Fast Electronics Group***

# Description and Requirements
## for the
# VXS Crate Trigger Processor Module
## D00000-16-08-S001

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## 1.0 Introduction

The development of a high speed sixteen channel 250 Msps Flash ADC (FADC) has been completed. These ADC modules have been designed on a 6U "B" size VME64x module format that uses the serial extensions as defined in VITA 41 or VXS[1]. The Flash ADC-250 will be used by many detector subsystems proposed for 12GeV experiments. These experiments will require a level 1 trigger system, and the input signals that drive these front end Flash ADC modules, will produce the first stage of the level 1 trigger signal chain.

The signals from FADC-250 module will be processed by a central Crate Trigger Processor (CTP). The Crate Trigger Processor is designed in conformance with the VITA 41 switch slot specification, and will manage the high speed serial connections from each VXS payload module in the crate.

A Jefferson Lab VXS crate will be configured to use up to sixteen (16) FADC-250 modules. Each of the sixteen (16) FADC-250 modules will transfer data to the central Crate Trigger Processor. The Crate Trigger Processor will can be configured to run in at least three processing modes depending on what type of detector is connected to the FADC-250 modules. For example, in a Time-Of-Flight (TOF) application, the counters can be configured so that the Crate Trigger Processor produces a track count output. The 'Track Count' data output is sent to the Level 1 Sub-System Processor to become part of the Level 1 Trigger decision.

## 2.0 Purpose of the module

The Crate Trigger Processor module will be built as the "A" switch card as specified in VITA 41. The Crate Trigger Processor module is mechanically similar to a 6U, "B" size VME64x module, with a significant difference in the backplane connection scheme. This module will use the backplane connectors and signal definitions as specified in VITA 41 for the "A" switch card.

One of the main functions of the Crate Trigger Processor is an energy sum function, which collects the sum value from each Flash ADC-250 module within the crate using the high speed point to point connections from each (payload) slot. As defined in the VITA 41 specification, each payload port(slot) has eight (8) differential pairs that connect to the switch "A" slot. The Jefferson Lab VXS crate will be configured as a redundant "Star" backplane, which means two switch slots will be available, but for the purpose of this document, only the "A" switch slot will be detailed. Definitions for connections to the VXS "B" switch will be included because these signals are critical to the design and functionality of the Crate Trigger Processor module.

## 3.0 Functional Description [Block Diagram]

A VITA 41 switch slot module is shown in Figure 1. Note the high speed multi-gigabit connectors used for the point to point signals from payload modules to the switch card. The switch slot module only receives +5V power from the VXS backplane, and there are two mechanical alignment keys that are required for the module that facilitate the proper mating between the board connectors and the backplane connectors.

Figure 2 shows how the payload 'slots' are logically connected to the "A" switch slot. The Jefferson Lab VXS Crate Trigger Processor module shall be designed to accept all eight (8) differential pairs from each payload port. Note that payload ports 17 and 18 will be dedicated to specific modules, so the Jlab VXS Crate Trigger Processor module will only use the first two(2) differential pairs from these payload ports.

Three Xilinx Virtex5 FPGAs provide the processing power for the CTP. Each Virtex5 XC5VLX50 handles data from five FADC and one Virtex5 XC5VLX110 handles

data from six FADC. The physical link between the CTP and the FADC is Xilinx RocketIO GTP Transceiver. The XC5VLX50 can either preprocess the data or pass the data without processing to the XC5VLX110 for further processing. There are 80 differential pair's connections from each XC5VLX50 to XC5VLX110 to accommodate the passing of unprocessed data from five FADC (5 FADC x 16 bits of data per FADC). The XC5VLX110 with 110,592 Logic Cell (see Xilinx Product Selection Guide for complete resource) can handle many processing algorithm. If more resources are needed, the XC5VLX110 can be replaced with XC5VLX155 with 155,648 Logic Cell. After processing data, the XC5VLX110 can pass the result to upstream module (Global Trigger Processor) via HFBR-7934Z Fiber Optic Transceiver. The HFBR-7934Z contains four transmit and four receive channels at 3.125 Gb/s 8B/10B encoded per channel.

The CTP module receives command and provides board status using ISquareC protocol to PayLoad Port 18. An Atmel High Performance, Low-power 8-bit 128L Microcontroller will manage the ISquareC protocol. The Atmel Microcontroller will communicate with the three Virtex5 FPGAs through an asynchronous bus.

The CTP module can be clocked from an on-board (250MHz) oscillator, LVPECL clock input at the front panel connector, or LVPECL differential clock from the Signal Distribution (SD) module. Clock that drives the GTP can either be 125MHz to support 3.125 Gbits or 250MHz to support 2.5 Gbits serial links. Clock selection is made through the microcontroller which decodes the commands from the ISquareC source module. The clock tree drives the Virtex5 GTP Transceiver and global clock pins. Both 250MHz and 125MHz clocks are available at the global clock pins. Two additional clock sources are 50MHz, for processing that does not have to be clocked at 250 MHz, and Auxiliary Clock that is used to initialize the GTP Transceiver and

The CTP receives a differential clock signal from the SD(Signal Distribution) module, and also includes the following connections between the SD and CTP modules: one LVDS (Sync), two LVTTL inputs, and two LVTTL outputs.

FPGA configuration data are stored in a Xilinx PROM. The PROM is programmable using JTAG and the JTAG connector is available at the front panel for code change in the field. In addition, the following features are at the front panel: eight LED to provide the status of the module, reset switch to reset the module, LVDS differential output (TRIGGER OUT).

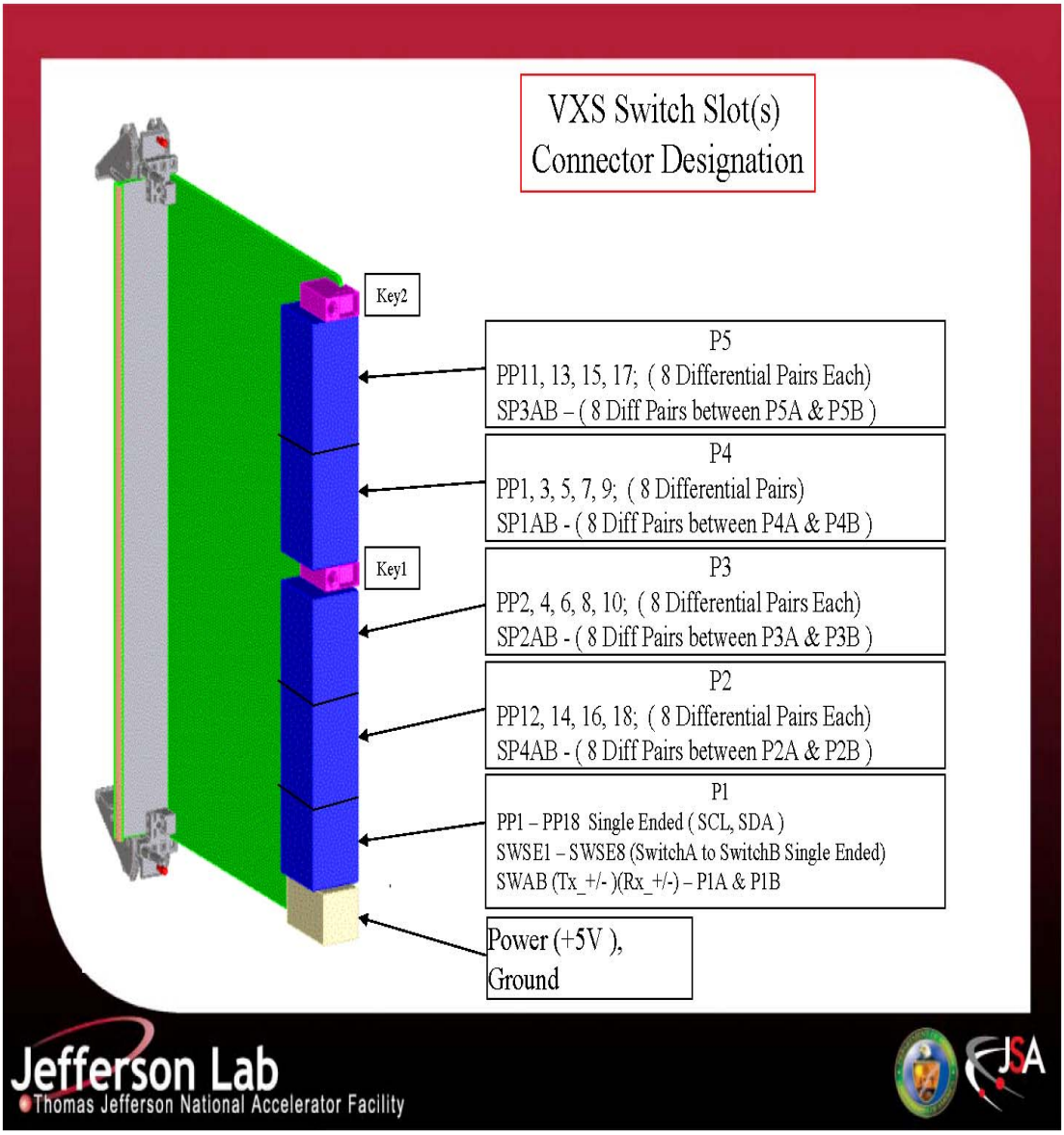



**Figure 1 – VXS Switch**

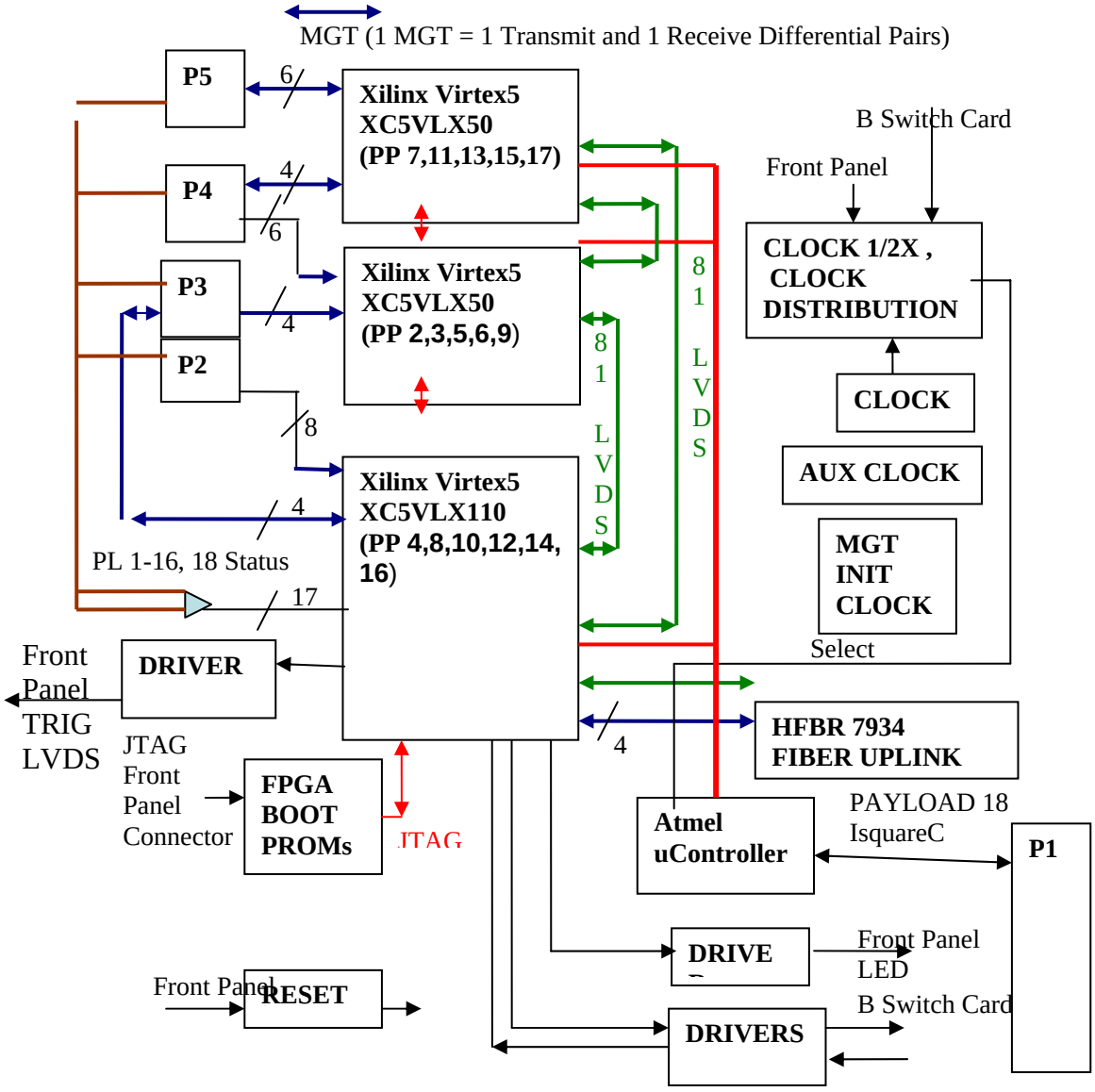
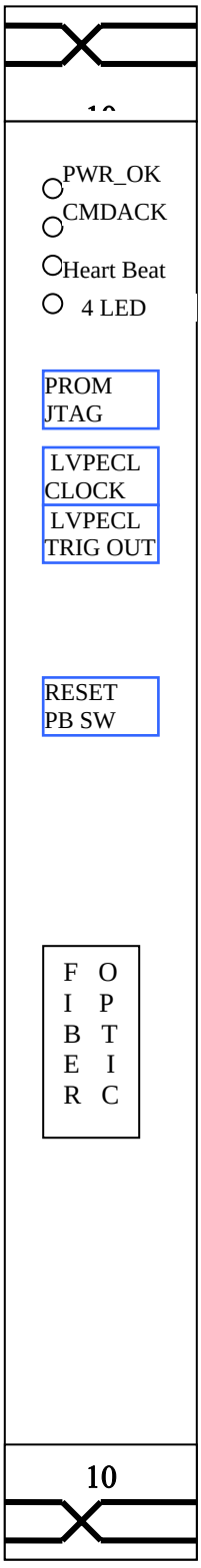



**Figure 2:** **PAYLOAD (Logical) PORT mapping to Jlab VXS Energy Sum Module.**
**Note: 1 GigaBit Tranceiver "Lane" equals 2 pairs. Total lanes == 70**

## Specification Sheet




MECHANICAL
- Single width VITA 41 “A” Switch Module

HIGH SPEED SERIAL INPUTS: ( P2, P3, P4, P5 )
- Supports up to two **G**igabit **T**ranceivers (GTP) from 16 payload module(full duplex)
- **G**igabit **T**ranceivers use CML logic levels between Xilinx GT devices.
- Supports GT Aurora links upto @3.125 Gbps
- Xilinx Virtex 5 FPGA Processors

CLOCK INPUTS
- VXS backplane LVPECL clock received from “B” switch
- Front Panel LVPECL CLOCK
- On Board 250 MHz Clock
- On Board 50 MHz Clock for GTP
- On Board Aux Clock

OUTPUTS: (Front Panel)
- Multi-Fiber Optic transceiver
  - HFBR-7934
  - POP4 compliant 4 channel Rx/Tx fiber module
- LVPECL TRIG OUT

MISCELLANEOUS IO
- LVPECL Input from “B” switch
- 2 LVTTL Input from “B” switch
- 2 LVTTL Output to “B” switch
- LVPECL Input from Payload 18

INDICATORS: (Front Panel)
- Power OK – Green LED
- Command Acknowledge – Green LED
- Module Heart Beat
- Four General Purpose Green LED

PROGRAMMING:
- On board JTAG Port to program FPGA
- Front Panel JTAG Port to program FPGA Config PROM
- Serial commands from Payload Port 18 ( $I^2C$ from Trigger Interface ). Atmel 128L uProcessor handles the protocol. Gateway for command and status.

## 4.0 Detailed Firmware Description and Requirements

1. **Payload input pairs:**

   The VXS Crate Trigger Processor module will use Xilinx Virtex 5 components to interface the high speed serial data from each payload module. The high speed serial data contains the sum value of sixteen ADC channels. The sum value is computed every 4ns on each payload module and transmitted to the crate sum module.

   The high speed serial transmission protocol will be Xilinx's Aurora, and the crate sum module must manage all payload input pairs using this method.

2. **Energy Sum Processing (ES)**
   - The crate sum module collects the sum value from each payload module in the crate and computes the total sum. The crate sum total is computed and the value is organized with time stamp data, formatted in the framing method outlined in the Sub-System Processor(SSP) uplink definition, and transmitted via a fiber optic transceiver. The crate sum module must be able to manage the( need words here to describe serial input skew differences etc)
   - The crate sum module will provide programmable comparator threshold values for a minimum and maximum sum value.
3. **Hit Bit Processing (HB)**
   - Collect Hit Bit data from individual FADC250 modules and perform combinatorial or other logic functions on the hit bits gathered from each payload module.
4. **Track Count Processing (TC)**
   - Collect track count data from each FADC-250 module and assemble this data to represent the total number of tracks that were processed from a specific detector such as scintillation counters
5. **Clock counter (Time Stamp)**
   - Each processing mode (ES, HB, TC), the crate sum module will provide a 48 bit clock counter value that records the number of clock pulses after a ~~reset~~ sync command is issued. This time stamp value is transmitted along with the total sum value over fiber optic cable to the Energy Sum Processor.
6. **Output Data Format**
   - Each processing mode (ES, HB, TC), the output data and uplink framing format to the **Sub-System Processor** is defined in the SSP specification document. The SSP document is included in Appendix N for reference.
7. **Transition Delay**
   - Each processing mode (ES, HB, TC), the total propagation delay for payload sum data to be transferred to the ~~total sum~~ output stage is (25 clock cycles?) 100ns.
8. **Reprogrammable**
   - Owing to the limited resource of the FPGA on the CTP module, only one processing mode can be stored and be executed at a time.

## 4.1- 4.6 Trigger Processing Modes: Functional Description and Requirements

Here is where the text goes to describe the three different processing modes (It will be filled out when the firmware is written) :

4.1. Energy Summing :
4.2. “Hit Bit” processing:
4.3. Track Count processing: .

## 5.0 Programming Requirements
## Command, Status and Configuration Registers

The VXS Crate Sum module receives programming commands via $I^2C$. The $I^2C$ bus master will reside in payload port 18(slot 20) of the VXS crate. Programming the VXS Crate Sum module includes the following sections:

1. **Energy Sum Processing:**
    - Configuration Register R/W:
        i. Select Clock Source
        ii. Reset
    - Mask Pay Load Registers R/W
    - Total Sum Threshold R/W
        - Value
    - Status Registers R
        - Clock Count
        - Serial Lane Status
        - FPGA Temperature Alarms
        - FPGA Vint, Vaux Alarms
        - Board 2.5V, 3.3V_FIBER Alarms.
        - Fiber Status
    - First LX50 FPGA die temperature in Celsius Status Register R
    - First LX50 FPGA die temperature in Celsius Status Register R
    - LX110 FPGA die temperature in Celsius Status Register
    - **TBD**

2. **Hit Bit Processing:**
    - Configuration Register R/W:
        i. Select Clock Source
        ii. Reset
    - Mask Hit Bit R/W
    - Status Registers R
        - Clock Count
        - Serial Lane Status
        - FPGA Temperature Alarms
        - FPGA Vint, Vaux Alarms
        - Board 2.5V, 3.3V_FIBER Alarms.
        - Fiber Status
    - First LX50 FPGA die temperature in Celsius Status Register R
    - First LX50 FPGA die temperature in Celsius Status Register R
    - LX110 FPGA die temperature in Celsius Status Register
    - **TBD**

3. **Track Count Processing:**
    - Configuration Register R/W:
        i. Select Clock Source
        ii. Reset

- Status Registers R
    - Clock Count
    - Serial Lane Status
    - FPGA Temperature Alarms
    - FPGA Vint, Vaux Alarms
    - Board 2.5V, 3.3V_FIBER Alarms.
    - Fiber Status
- First LX50 FPGA die temperature in Celsius Status Register R
- First LX50 FPGA die temperature in Celsius Status Register R
- LX110 FPGA die temperature in Celsius Status Register R
- **TBD**

## 6.0 Power Supply and Current Consumption

Only +5.0 Vdc is provided to the VXS Crate Sum module from the backplane. Maximum current capability for the power connector is 40 AMP. CTP estimated current consumption is 13 Amp. The module shall use an input protection fuse with the proper over-current rating.

The +5.0 VDC is regulated down to 3.3V, 2.5V, 1.8V, 1.2V, and 1.0V. Table 1 lists the approximate current consumption for the different voltages.

| DC Voltage | Current (Amps) | |
|---|---|---|
| + 3.3 V | 2 | Regulators |
| +2.5V | 1 | Regulators |
| +1.8V | .2 | Regulators |
| +1.2V | 3.6 | Regulators |
| 1.0V | 6 | |
| | | |
| SUM | ~13 | +5.0 Vdc BackPlane |

Table 1

[1] Flash ADC specifications and requirements